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SMALL STRUCTURES AND SUPERLATTICES FOR FUTURE HIGH-SPEED DEVICES

From: November 15, 1983 To: October 1, 1986

PREPARED BY
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PASADENA, CALIFORNIA

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ANNUAL TECHNICAL REPORT
TO
DEFENSE ADVANCED RESEARCH PROJECTS AGENCY

SMALL STRUCTURES AND SUPERLATTICES
FOR
FUTURE HIGH-SPEED DEVICES

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ABSTRACT

We report on our studies of novel microstructures for high-speed and high-density electronics. We have proposed and done simulations on five new three-terminal devices. We have had success in fabricating one of these new device structures and have measured the DC current-voltage characteristics. The desired three-terminal device behavior has been observed at **300K and 77K**. We are in the process of attempting to fabricate the other devices now. We have completed the installation of a picosecond pulser and are in the process of obtaining some of the first measurements of the response time of tunneling devices. We have developed a capability to simulate the process of making high-speed measurements with micro-strip lines. This simulation capability will be essential in interpreting the results of the high-speed measurements. We investigated the properties of silicide-silicon interfaces that could have application in high-speed, high-density devices. In particular, we have made measurements of the Schottky barriers on $NiSi_2$ on Si and studied the transport via tunneling across the $NiSi_2$-Si and $CoSi_2$-Si interfaces. We have completed the development of a small Si MBE growth chamber and are currently growing silicide-silicon structures in this system. We are in the process of installing a unique MBE facility that will include provision for growing group IV semiconductors and silicides, III-V semiconductors, analyzing structures, using Auger and ESCA, and a metallization chamber that includes not only the provision for evaporating metals but can be used as an intro-chamber for a more extensive processing facility. This facility is unique in the world but is serving as a prototype for systems planned by other groups. We have carried out some basic studies of the properties of GaAs-GaAlAs interfaces that are basic to their use in novel device structures.

I. Introduction

Small structures of high-speed and perhaps high-density electronic devices have become quite an important topic of research since this program was started three years ago. Research activities, particularly at a number of the Japanese companies, including Hitachi, Fijitsu, NEC, are aimed at producing high-speed, high-density electronics based on using tiny structures. Work in this country is confined to a relatively small number of sub-critical industrial research activities, notably at TI and IBM, and a few university research efforts, notably at the University of Illinois and Caltech. The Caltech activity is supported primarily under the funding provided by this contract.

In the original proposal, we stressed the importance of establishing a program to study novel electronic structures both in III-V's and group IV semiconductors.

The funding provided by the DARPA program was to establish a facility at Caltech to fabricate these structures, and to carry out an experimental and a theoretical program to determine the properties of these structures. This activity is on-going and is beginning to yield exciting results. Currently, these approaches to devices are very promising. For the United States to maintain a viable competitive position *vis-a-vis* the Japanese, it is essential that these activities be continued.

The original program included a number of major research goals. These included (as quoted from the original proposal):

- Develop small structures and superlattices for application in a broad range of electronic and optical devices.
- Develop superlattices for high-speed electronic applications. For example, the zone folding superlattices could be used to suppress the intervalley scattering and, hence, enhance the drift velocity.
- Develop thin layers as control structures in high-speed devices.

- Develop small structures, consisting of silicides and silicon, for numerous device applications.
- Study the transient response of small structures to evaluate their potential for application in high-speed devices.
- Utilize unique computer program to search for new epitaxial systems.

To accomplish these major research aims, a program with a number of tasks was proposed including: experimental determination of the properties of small structures; thin control layers in high-speed devices; theory of properties of small structures; transient phenomena in small structures; small structures formed from silicides and silicon; search for new epitaxial systems. Major progress has been made in establishing the research facility and in pursuing these various research goals along the programmatic directions indicated by the topics of the various research tasks.

II. Progress on the Program

A. Establishment of Facility for Fabricating and Studying Small Structures

Four major facilities were to be established under the funding provided by this program–a lithography facility, a molecular beam epitaxy and surface analysis facility, a picosecond pulse facility, and an up-grade to the computer facility to allow more extensive simulations.

A lithography facility, consisting of laminar flow hoods, contact mask aligner, microscopes, spinners and furnaces, has been in place for over two years and is a key part of the activities in the group now. All device fabrication in the group takes advantage of this facility. Some of the successes that we have reported below are due to the dedicated nature of this specialized facility for doing research in electronic devices. We are at the present time in the process of installing a reactive

ion etcher that was purchased under this contract. This etcher will give us more capability at defining small structures for making both three-terminal devices as well as two-terminal.

The picosecond pulse facility has been in operation for approximately one year. We are in the process of making detailed calibrations between our facility and the one at Los Alamos of which it is an exact copy.

The up-grade to the computer facility was carried out approximately two years ago. This included the addition of a graphics terminal, conversion of our VAX 11/780 into a 11/785 with approximately a 70 percent increase in performance, the addition of memory to improve overall system performance, plus the addition of some disk drives to increase the size of the scratch files that we could produce during calculations. This facility has played a key role in obtaining many of the results shown in the detailed report of our progress in the experimental and theoretical program.

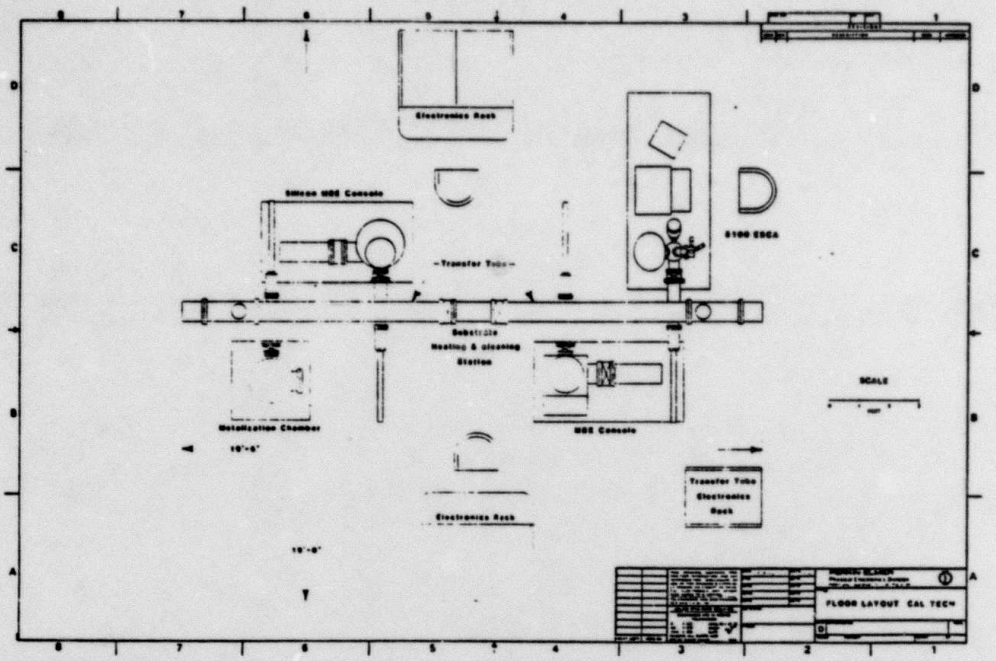

Figure 1. A schematic of the layout of the Caltech MBE facility purchased in part by this program. The facility is unique in that it combines growth facilities for III-V semiconductors with those for group IV semiconductors and silicides. Analytical measurements can be carried out in a special surface analysis facility. A special metallization chamber includes the capability of evaporating metal layers and acts as an intro-chamber for a potential processing facility.

One major facility that was purchased under this program is being assembled and is becoming fully operational. This facility is a unique facility in the world for the fabrication of small structures and their evaluation, using surface analysis. We are at the present time installing a specially designed Perkin-Elmer Molecular Beam Epitaxy Machine in a clean room facility that will consist of roughly 1000 square feet of class 10,000 clean room with provisions for class 100 at points near the entry of the MBE machine. This facility took quite a long time to purchase, since none of the U.S. vendors, Perkin-Elmer MBE and Varian, were willing at first to bid on such a system. It was our determination that VG and Riber would be difficult for us to deal with, since they both had a reputation for relatively poor service in

the United States. Finally, after approximately a year and a half of negotiation, we were able to convince Perkin-Elmer to take total system responsibility for the system as shown in Fig 1. This system consists of a III-V growth chamber, a silicon-germanium-silicide growth chamber, a surface analysis facility with both ESCA and Auger, and a metallization chamber that can be used as a entry into a processesing line. For Perkin-Elmer to take on this system responsibility required a radical new approach in MBE machine design. Perkin-Elmer has committed itself to the design of modular MBE machines based on this order. They have also committed to the production of a silicon MBE growth chamber which they had not previously delivered. The surface analysis facility is unique in that the ESCA includes a monochrometer that will give the U.S. a capability in ESCA that apparently is better than other ESCA's available from abroad. From the time of our original purchase order with Perkin-Elmer, a number of these system have been sold, including systems for the University of Illinois and Purdue. Both of these are taking advantage of the modular approach pioneered by the Caltech program and the capability of mixing various growth chambers on the same MBE system. While this system is not fully operational, various components of the system will be in place shortly and we expect the III-V growth chamber, ESCA and Auger, and metallization chambers to be operational by the spring. The plans are being finalized for the silicon growth chamber now, and we expect delivery by the end of the summer.

It is difficult to over-stress the importance of the development of this modular approach and a combination of a number of growth chambers for different materials on the same system. Silicon MBE combined with III-V MBE shows real promise in producing a number of valuable electronic devices. For example, recent success in growing GaAs directly on silicon using MBE has very large device implications. With the system as shown in Fig. 1, it will be possible to grade silicon-germanium

alloy to germanium which would then lattice match directly with GaAs. Multi-layered structures, involving additional layers of silicon, could potentially be grown by grading silicon-germanium alloys back to silicon and then growing electronically useful layers of silicon. Mixed systems involving metals, silicon germanium alloys, GaAs and other III-V's, such as InAs, GaSb, and AlAs, as well as, mixed systems can be fabricated in such a facility. While we realize it has taken a great deal of time to put such a system together, we believe that the unique capabilities provided by this system will give both the United States, Caltech and the DARPA Research Program a substantial lead in the research to find new and novel electronic devices that will put us in a competitive position with the Japanese in particular.

We have completed the construction of a small silicon MBE machine in our 12-inch Varian growth chamber. This machine will be used to fabricate small structures mainly of silicide and silicon. We are beginning to grow our own structures in this system. As the large silicon growth chamber comes on line, we will use the small machine to grow more exotic silicon-silicide structures that might contaminate the big system.

B. Progress on Research Objectives

One of the key aspects of the research program, as proposed, is the study and exploration of novel two- and three-terminal devices that can be used for both high-speed and high-density devices. While most of the research programs to date have concentrated on two-terminal devices, we realize that the real payoff will come with the development of a viable three-terminal device. To this aim, we have proposed five new three-terminal devices based on tunneling. One of these, the so-called "Stark" transistor, involves the use of tunneling into the sub-bands whose positions are modulated by an electric field to produce transistor-like characteristics. A device of this type is shown schematically in Fig. 2. A simulated current-voltage

characteristic for such a device is contained in Fig. 3. The proposal for this device structures has been published in Applied Physics Letters. The paper is included in the Appendix as paper 1.

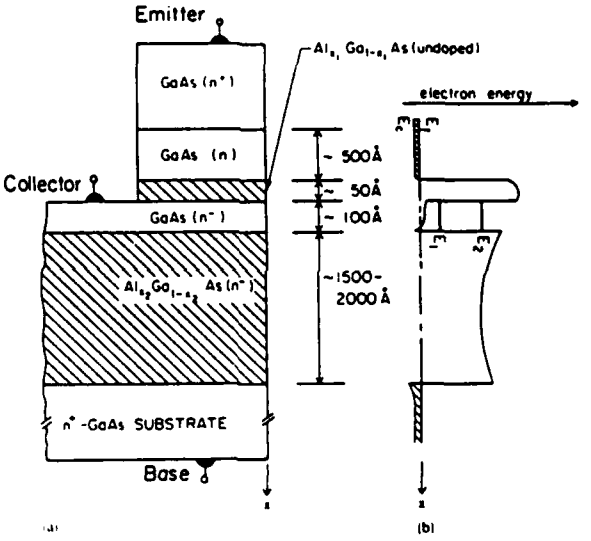

Figure 2. (a) Schematic diagram of a "Stark" transistor fabricated in the GaAs-GaAlAs technology. (b) The conduction band edges in the device. Transistor action is obtained by modulating the position of the sub-bands in the quantum well with electric fields produced by the gate (electrode at the bottom).

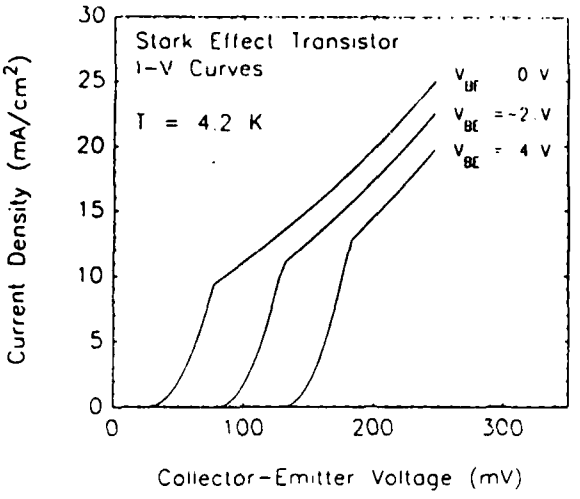

Figure 3. Theoretical current-voltage characteristics of a "Stark" transistor. We have plotted the current density between the emitter and collector as a function of the emitter-collector bias. The curves are parameterized by the base-emitter bias.

We have also investigated the integration of the negative-resistance characteristics obtained from double-barrier tunnel structures with various standard semiconductor devices to produce controllable negative resistances. Devices of this type could be used in circuits for phase arrayed high-frequency oscillators, as well as high-density logic circuits. Devices that have been incorporated include the vertical FET, the standard MESFET, and the permeable based transistor. A schematic of one of these devices, the tunnel emitter integrated with a vertical FET, is shown in Fig. 4. The proposals for these various devices are discussed in more detail in the published papers that have been attached in the appendix. These particular devices are considered in paper 2.

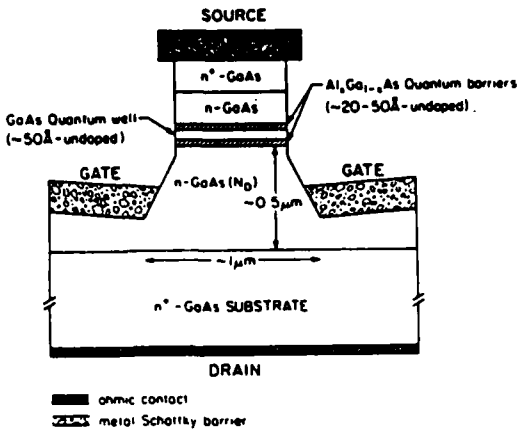

Figure 4. A schematic of a vertical FET integrated with a tunneling emitter. Application of a voltage to the control gates changes the resistance in series with the negative resistance due to the resonant tunneling emitter and, hence, shifts the position of the negative resistance.

Recently, we have had success in fabricating three-terminal devices based on tunneling. In Fig. 4, we have the current-voltage characteristics measured for a vertical FET integrated with a negative-resistance tunnel structure. In this figure, one can see that the negative-resistance structure is modulated by changing the voltage on the control electrode.

Other devices are currently under exploration including attempts to fabricate the "Stark" transistor. Recently, in a sequence of articles in Applied Physics Letters (by authors in the US and Japan) most of the basic concepts of the "Stark" transistor have been demonstrated, and it seems likely that we will have a success once we get our processing techniques under control for the fabrication of such devices.

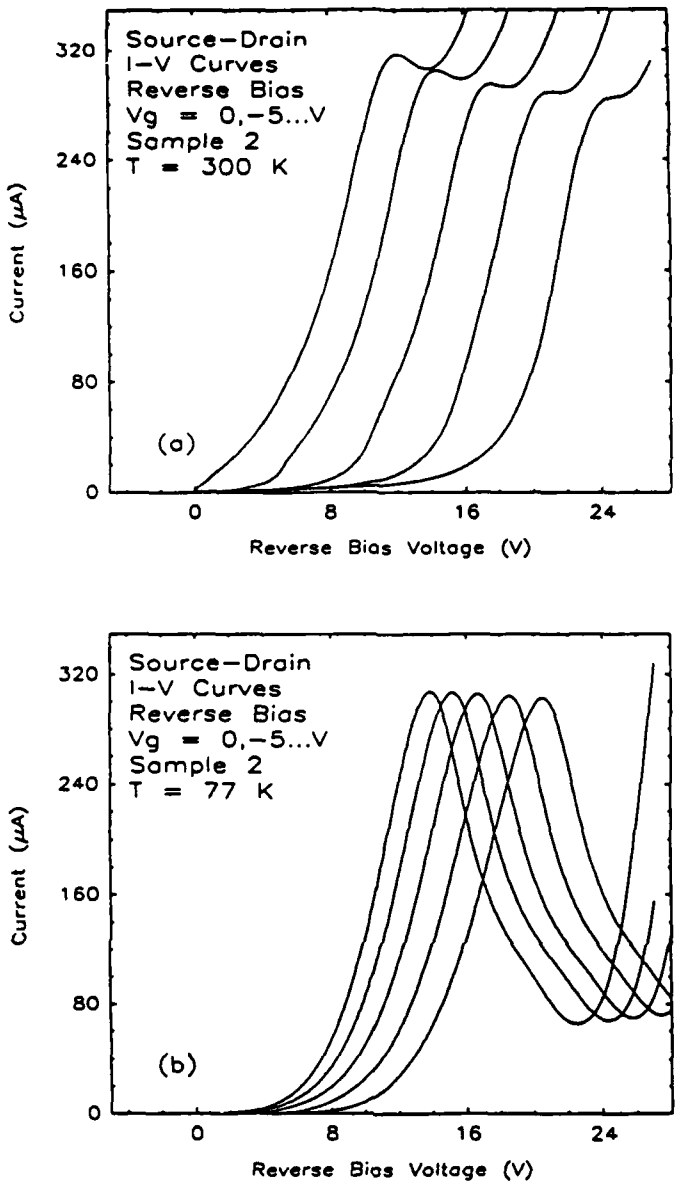

Figure 5. Experimental current-voltage characteristics of a device consisting of a tunnel emitter integrated with a vertical FET. The data shown were taken at **room temperature**, the upper curve and liquid nitrogen temperatures, the lower curve. We have plotted the source-drain current as a function of the source drain-bias for different values of the gate voltage.

A study of high-speed devices requires serious measurements of the phenomena at high speeds. One of the key components of our research program has been the development of the picosecond pulse facility plus the capability to simulate the

measurement of high-speed phenomena, using numerical simulation. We are directly transferring the technology for making high-speed measurements from the group at Los Alamos under the direction of Bob Hammond. We have a great deal of progress in making measurements of these important phenomena. We have completed a computer program for simulating the behavior of micro-strip lines under realistic conditions including: the launching of the picosecond pulse, the interaction of the pulse with high-speed device, and the detection of the pulse. As far as we are aware, this capability is unique in that other groups have not explored in detail the spatial as well as time dispersion of the pulses along micro-strip lines. We have demonstrated in a sequence of experiments at Los Alamos that the photon controlled electronic switches, used to launch the electrical pulses on the micro-strip line from the picosecond pulses, will operate both at room temperature and low temperature. We have designed packaging structures for putting both the two-terminal tunnel structures along with micro strip lines together in an integrated *package for measurement* both at Caltech and Los Alamos. At this very moment, experiments are going on at Los Alamos to make the first test on these structures. The use of the Los Alamos facility to help calibrate our facility will guarantee that when results begin to come from our picosecond pulser, we will not have to go up a learning curve of developing a credibility for our experimental technique. We expect to have results measuring the transient response of tunnel structures within the next few months.

One of the major directions of the original proposal was to explore the possibility of using silicon, silicides and silicon-germanium in novel electronic structures. To this end, we have been studying the properties of silicon-silicide structures where the silicide is single crystal and epitaxial on the silicon. A second layer of silicon could be grown on top of the silicide. Two such systems are $NiSi_2$ and $CoSi_2$ on silicon. Metal-base transistors and permeable-base transistors based on these system

have been fabricated in this country at GE and AT&T Bell Laboratories as well as in France and almost assuredly in Japan. In particular, we have been concentrating on trying to understand the transport across the metal semiconductor interface and that is the silicide-silicon interface. With this aim in mind, we have been exploring the properties of the Schottky barriers formed between the silicide and silicon. The results of this study are contained in a sequence of papers which are included in the appendix as papers number 3, 4, and 5. The $NiSi_2$ forms in A and B orientations. Results of photoresponse measurements indicate that the barrier heights for type A and type B orientation differ by approximately 100 meV. This result found by other investigators as well suggests that the details of the atomic structure at the interface could play a role in determining the Schottky barrier. Another very important issue with respect to the formation of silicides-silicon microstructures is the question of thermal stability of the transition metal silicide against the silicon. Processing temperatures and device structures will in part be determined by the degree of thermal stability attainable at these interfaces. In paper 6, we reported on the results of a study of the thermal stability of silicon-silicide Schottky barriers on silicon. These results indicate in the case of NiSi on silicon that it is likely that we will be able to fabricate structures up to temperatures on the order of 500C. However, their samples did not involve the epitaxial silicides which we are now investigating for device applications. We plan to reproduce those experiments to see if the epitaxial silicides are stable to higher temperatures. We expect that they will be.

To assess in more detail the character of the transport between epitaxial silicides and silicon, we have been studying tunnel structures consisting of epitaxial silicide layers on a silicon substrate. Study of the tunnelling characteristics of these systems has given us information on the kinds of phenomena that govern this transport. Since most of the proposed device structures, involving silicon and silicides, involve

transport of this type, this fundamental study is of importance in assessing the possibilities for these materials in potentially high-speed devices. The results of this study are contained in paper 7.

As a basic part of our exploration of potential high-speed and/or high-density device phenomena we have been studying the basic properties of GaAs-GaAlAs heterojunctions. Current-voltage and photo-response measurements on these heterostructures have given us information on trap densities and the possibilities for establishing inversion layers at these interfaces. The results of these studies are published in a sequence of papers which have been attached in the appendix as papers 8, 9, 10 and 11.

III. Students Supported under this Program and Ph.D's Awarded

A number of students have already been supported in part under this program. These include:

STUDENT	STATUS
R. T. Collins	Ph.D. 1984 Currently member of technical staff at IBM T. J. Watson Research Center
A. Prabhakar	Ph. D. 1984 Currently program manager DARPA
R. Hauenstein	Ph. D. expected Fall 1986
A. Bonnefoi	Ph. D. expected Fall 1986
M. Johnson	Ph. D. expected Summer 1987
T. Woodward	Completed Ph. D. candidacy examination
D. Chow	Third year graduate student in Applied Physics

IV. Major Trusts in the Next Research Period

Some of the major activities we expect to come to fruition during the next research period include: bringing into operation the MBE facility, completion of some of the first transient measurements on tunnel structures, exploration of silicon-silicide growth in our new small silicon MBE machine and successful fabrication of three-terminal devices including a "Stark" transistor. We expect that this program, if continued to be funded will provide important activities in the general direction of producing high-speed, high-density devices for incorporation in the next generation of electronics.

APPENDIX

PAPERS PUBLISHED WITH THE SUPPORT OF THIS PROGRAM

Inverted base-collector tunnel transistors

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(Received 1 July 1985; accepted for publication 7 August 1985)

Two novel three-terminal devices based on tunneling in quantum well and quantum barrier heterostructures are proposed and analyzed theoretically. In both devices, the relative positions of the base and collector are interchanged from conventional emitter-base-collector sequence. This provides a means for obtaining negligible base currents and large current transfer ratios. In both cases, a base voltage controls the emitter-collector tunneling current by shifting the resonances in a quantum well. Calculations indicate that significant variations in the emitter-collector current-voltage characteristics can be obtained for reasonable base-emitter voltages. We call the two devices a Stark effect transistor and a negative resistance Stark effect transistor, respectively.

Electronic tunnel structures are a source of increasing interest. Two-terminal devices based on tunneling in single and double barrier heterostructures have been studied.[1-9] While it is true that these two-terminal structures have a number of potential applications, three-terminal devices would be preferable in many cases.

The idea of making three-terminal devices based on tunneling was pioneered in 1960 by Mead.[10] He proposed a metal-insulator-metal-insulator-metal hot-electron transistor. A number of devices based on this concept have been proposed and investigated experimentally.[11-13] All of these structures suffer from very small emitter-collector current transfer ratios due to large base currents.

Recently, Jogai and Wang[14] calculated the tunneling current for a conceptual three-terminal, double barrier device consisting of alternating layers of GaAs and $Al_xGa_{1-x}As$, forming the emitter, base, and collector. They proposed a configuration in which the base contact would be made to the GaAs quantum well and the two barriers independently biased. A highly conductive base was required so that a potential could be applied to it, but no base current was allowed to flow. This is a somewhat unphysical and unrealistic assumption. In addition, varying the collector-base voltage did not produce very significant changes in the device current-voltage characteristics.

In this letter, we propose and analyze two three-terminal devices which we expect to have reduced base currents and improved device performances. Although other semiconductors could be used, the devices are presented here in the context of $GaAs/Al_xGa_{1-x}As$ heterojunction technology. Since tunneling is the main current transport mechanism, these devices should feature the high-speed characteristics associated with tunnel structures. They should also have large emitter-collector current transfer ratios. The key step in achieving this goal is to interchange the relative positions of the base and collector, thus locating the latter in the region where current is most likely to flow. Figure 1 shows schematically the first proposed structure, together with its energy-band diagram at equilibrium. The emitter is an n-type GaAs layer. Doping concentrations on the order of 5×10^{16}–5×10^{17} cm^{-3} should provide sufficient tunneling currents and, at the same time, allow resonant tunneling effects to be observed at room temperature.[9] The emitter is followed by a thin undoped $Al_{x_1}Ga_{1-x_1}As$ tunneling barrier and a lightly doped n-type quantum well. The collector contact is made to the well. Alloys which give shallow and abrupt ohmic contacts, such as Au/Ge-Ag-Au or Au/Ge-Au-WSi for example, should be used. The next layer is lightly doped $Al_{x_2}Ga_{1-x_2}As$ barrier, sufficiently thick to prevent electrons from tunneling through it. In addition, an alloy with large Al composition is desirable to minimize thermionic emission over the barrier. Finally, a heavily doped n-type GaAs substrate serves as the base electrode.

The principle of operation of the proposed device is described below. First, let us consider the case in which no base voltage is applied. When the collector is biased positively with respect to the emitter, electrons near the Fermi level in the emitter tunnel through the thin $Al_{x_1}Ga_{1-x_1}As$ barrier into the collector. As long as the emitter Fermi level remains below the first subband in the well, a negligible tunneling current is expected. When the bias voltage is such that the emitter Fermi level reaches the first subband, the current is significantly increased. The current-voltage (I-V) characteristics should thus feature enhancements corresponding to the alignment of the emitter Fermi level with each resonance in the well. If a potential difference is now applied between

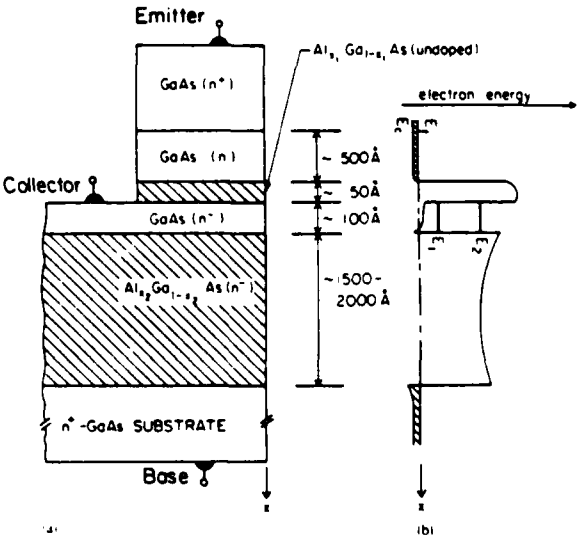

FIG. 1. Schematic diagrams (not to scale) of (a) a cross section of the proposed Stark effect transistor (SET), (b) the conduction-band edge at equilibrium as a function of position in the x direction (perpendicular to the layers).

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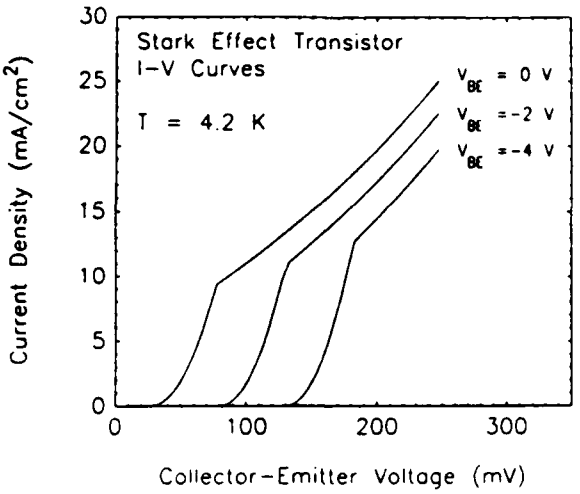

FIG. 2. Calculated current-voltage characteristics for the Stark effect transistor (SET). The barriers are pure AlAs, 50 and 1000 Å thick, respectively. The well is a 50-Å-thick GaAs layer. The conduction-band offset is taken to be 0.96 eV.

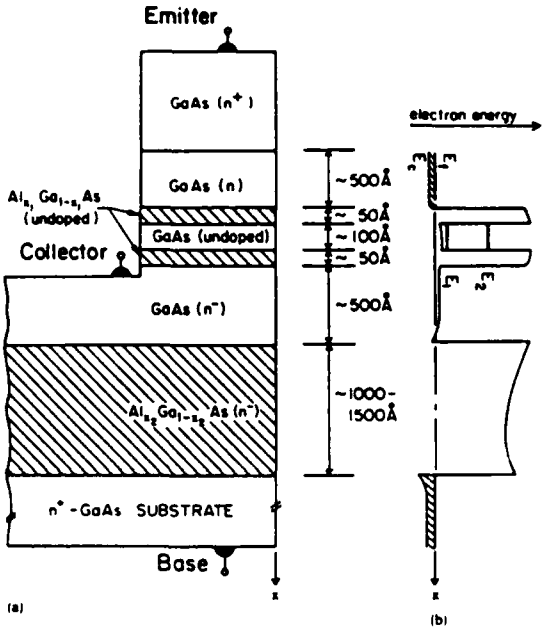

FIG. 3. Schematic diagrams (not to scale) of (a) a cross section of the proposed negative resistance Stark effect transistor (NERSET); (b) the conduction-band edge at equilibrium as a function of position in the x direction (perpendicular to the layers).

the base and emitter, an electric field perpendicular to the layers is created. The field will modify the positions of the subbands in the well with respect to the emitter Fermi level and thus modulate the tunneling current. The field will penetrate into the quantum well region for the following reasons: (i) the barriers and well are lightly doped; (ii) the $Al_{x_1} Ga_{1-x_1} As$ barrier is not thick enough to drop all of the base-emitter voltage; (iii) the device geometry is such that the collector contact does not completely shield the emitter from the base.

Theoretical I-V characteristics for the device are shown in Fig. 2. These curves were calculated using Bardeen's many-particle tunneling formalism.[15] In this approach, which starts from Fermi's Golden Rule, the density of finals states, ρ_f, appears explicitly in the calculation. In the present case, ρ_f is simply a sum of step functions since each resonance in the well is the bottom of a two-dimensional energy band. The matrix element was calculated by using WKB wave functions in the barrier region. A two-band model, $\mathbf{k}\cdot\mathbf{p}$ theory calculation was used to obtain the complex band structure in the barrier. Because the barriers and well are lightly doped, the base-emitter voltage V_{BE} was assumed to drop linearly in those regions. The calculated curves display the substantial variations of the emitter-collector I-V characteristics which may be obtained by modulating V_{BE}. Base-emitter voltages much higher than those needed to produce significant transistor action can be applied without producing avalanche breakdowns. If V_{BE} is negative, the levels in the well are shifted upwards and a small negative current might flow to the emitter when V_{CE} is small. This is an additional incentive to make the well and the $Al_{x_1} Ga_{1-x_1} As$ barrier lightly doped.

The main advantage of this configuration is a negligible base current and thus a large current transfer ratio. Because the quasistationary states in the well are modulated by an electric field to produce transistor I-V characteristics, the proposed device could be called a Stark effect transistor (SET).

The transistor I-V characteristics described above can be modified and enhanced by adding a potential step in the GaAs well constituting the collector. The step can be a thin $Al_x Ga_{1-x} As$ layer with an Al composition smaller than that of the barriers. Its main effect is to modify the relative positions of the resonant states in the well. The structure can now be designed to obtain a certain energy spectrum or to produce given shifts of some of the subbands. This makes it possible to optimize device performance according to the requirements or applications.

To further illustrate the concept of subband modulation by means of an electric field applied from a controlling electrode, another device configuration is proposed. It is characterized by a resonant tunneling double barrier heterostructure. Such a device structure is shown schematically in Fig. 3, together with its energy-band diagram at equilibrium. This device operates on the same principle as the Stark effect transistor. The values of the fields and the shifts of the levels resulting from the base-emitter modulating voltage were estimated to be of the same order of magnitude as before. In this case, however, no contact needs to be made to the quantum well. The essential feature of this device configuration is the presence, in the emitter-collector I-V characteristics, of negative differential resistances controlled by the base-emitter voltage.

Theoretical I-V characteristics for the device are shown in Fig. 4. The approach of Vassell *et al.*[16] was used to calculate the tunneling current through the double barrier heterostructure separating the collector from the emitter. The base-emitter modulating voltage was once again assumed to drop linearly in each region. This device, which could be called a negative resistance Stark effect transistor (NERSET), offers several advantages over any double barrier configuration in which the base is located in the quantum well: (i) easier fabrication; (ii) no base current, and thus larger cur-

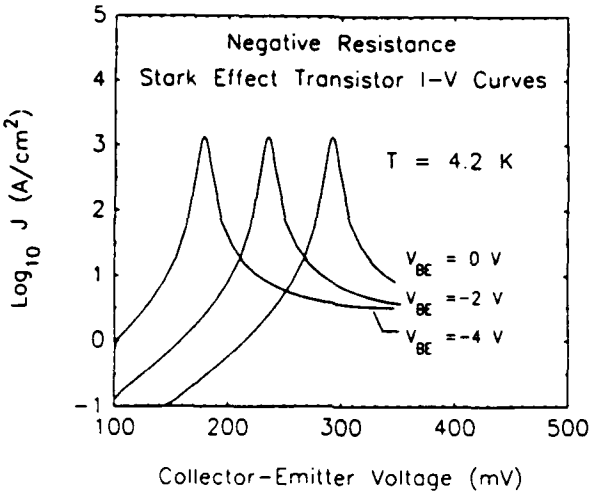

FIG. 4. Calculated current-voltage characteristics for the negative resistance Stark effect transistor (NERSET). The tunnel barriers are 20-Å-thick $Al_{0.4}Ga_{0.6}As$ layers and the well a 50-Å-thick GaAs layer. The conduction-band offset is taken to be 0.5 eV.

rent transfer ratios; (iii) undoped well; (iv) no transverse electric fields in the well which destroy the coherence of wave functions across the entire double barrier structure. These last two conditions are essential for optimum resonant tunneling.

In summary, we have proposed and analyzed two novel three-terminal devices based on tunneling in quantum well and quantum barrier heterostructures. Their main characteristic is that the relative positions of the collector and base electrodes have been interchanged with respect to the conventional emitter-base-collector sequence. This makes it possible to obtain negligible base currents and large current transfer ratios. Electric fields produced by applying a voltage to the base modulate the positions of the subband levels in the quantum well and thus control the emitter-collector tunneling current. Calculations showed that significant variations in the emitter-collector *I-V* characteristics can be obtained by modulating the base-emitter voltage. Although these devices were analyzed in the context of GaAs/$Al_xGa_{1-x}As$ heterojunction technology, other semiconductors could be used. Experiments are under way to measure the properties of these structures and to explore their applications in high-frequency analog and digital circuits.

John Lambe played a key role in calling our attention to the possible use of electric fields in changing the positions of subbands. A. Zur developed the computer programs used to calculate the *I-V* characteristics of the NERSET. M. B. Johnson, T. E. Schlesinger, T. K. Woodward, and G. Y. Wu have all helped us in the clarification of our thinking on these device concepts. This work was supported in part by the Defense Advanced Research Projects Agency under contract No. N00014-84-C-0083 and the Office of Naval Research under contract No. N00014-82-K-0556.

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Resonant Tunneling Transistors with Controllable Negative Differential Resistances

A. R. BONNEFOI, T. C. MCGILL, AND R. D. BURNHAM

PAPER 2

Abstract—**Three-terminal devices based on resonant tunneling through two quantum barriers separated by a quantum well are presented and analyzed theoretically. Each proposed device consists of a resonant tunneling double barrier heterostructure integrated with a Schottky barrier field-effect transistor configuration. The essential feature of these devices is the presence, in their output current-voltage ($I_D - V_D$) curves, of negative differential resistances controlled by a gate voltage. Because of the high-speed characteristics associated with tunnel structures, these devices could find applications in tunable millimeter-wave oscillators, negative resistance amplifiers, and high-speed digital circuits.**

ELECTRONIC devices based on tunneling are a source of increasing interest. In particular, resonant tunneling in structures made of two GaAs electrodes separated by two thin $Al_xGa_{1-x}As$ barriers and a quantum well have been extensively studied [1–6]. Two important properties of these double barrier heterostructures are (i) the presence of negative differential resistances in their current-voltage (I–V) characteristics, and (ii) expected operating frequencies in the terahertz range [2]. While it is true that these two-terminal tunnel structures have a number of potential applications, three-terminal devices would be preferable in many cases [7], [8].

In this letter, we propose and analyze three-terminal devices in which the current through a resonant tunneling double barrier heterostructure is modulated by a Schottky barrier gate placed along the path of the electrons. In fact, these devices can be viewed simply as tunnel structures integrated with Schottky barrier field-effect transistors (MESFET's). For small source-drain bias voltages, a MESFET operates in its linear mode and acts as a variable resistor controlled by the gate voltage. This property may be used to modulate the amplitude and position of the tunnel structure negative differential resistances. We could observe these effects by simply connecting one of our two-terminal tunnel structures [5] in series with a commercial FET. The I–V characteristics obtained in this simple test are shown in Fig. 1 as a direct demonstration of this concept. However, by integrating the FET and double-barrier heterostructure, dimensions can be reduced and parasitic resistances and noise minimized. These are essential requirements for high-frequency performance.

The first proposed device structure is shown schematically in Fig. 2. It consists of a resonant tunneling heterostructure integrated with a short channel MESFET. After tunneling through the quantum barriers and well, the flow of electrons is controlled by a Schottky barrier gate placed along a thin GaAs channel. The tunnel structure consists of two $Al_xGa_{1-x}As$ barriers, about 20–50-Å thick, separated by an undoped GaAs well, approximately 50-Å thick. For the top GaAs layer, donor concentrations of 5×10^{16}–5×10^{17} cm^{-3} should provide sufficient tunneling currents and, at the same time, allow resonant tunneling effects to be observed at room temperature [6]. Submicron microwave and millimeter-wave FET fabrication techniques can be used to form the gate and the source and drain ohmic contacts [9]–[13].

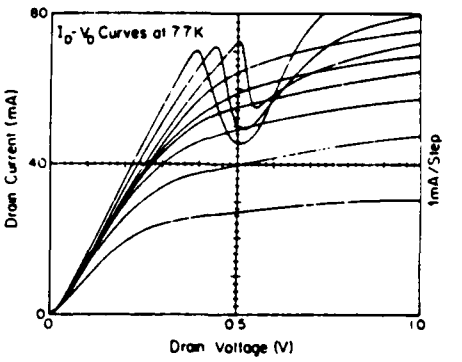

Fig. 1. Experimental I–V characteristics at 77K for a two-terminal resonant tunneling structure connected in series with a commercial n-channel enhancement-mode VMOS power FET.

Calculated output current-voltage ($I_D - V_D$) characteristics for the schematic of the device in Fig. 2 are shown in Fig. 3 for the first resonance. Because we are mainly interested in the linear regime of the FET, the two-region model of Pucel *et al.* [14] was used to obtain the velocity-field curve in the channel. For GaAs, this model has been shown to agree perfectly with two-dimensional analysis in the linear region, and to within ± 15 percent in the saturation region [15]. The characteristics of the tunnel structure constituting the source were obtained by measuring the I–V curves of two-terminal resonant tunneling heterostructures. The growth technique, preparation procedure, and properties of these two-terminal devices were discussed elsewhere [3], [5]. The structure corresponding to Fig. 3 had pure AlAs barriers, approximately 50-Å thick, and a nominally undoped GaAs quantum well, about 60-Å thick. The curves in Fig. 3 were calculated using a channel width a, of 0.20 μm, a gate length L, of 0.75 μm, and a gate width, perpendicular to the plane of Fig. 2, of 20 μm. The doping in

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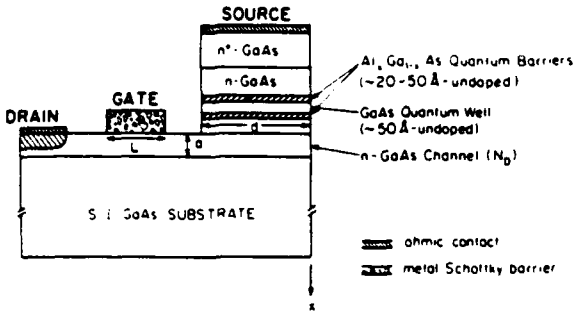

Fig. 2. Schematic diagram (not to scale) of a cross section of the first proposed transistor structure, the "Resonant Tunneling MESFET." The device can be symmetric with respect to the x-axis to minimize channel resistance.

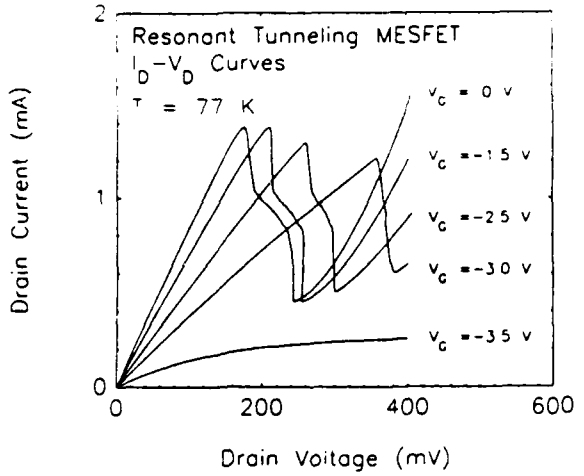

Fig. 3. Calculated current–voltage ($I_D - V_D$) characteristics in the voltage range 0–400 mV for the "Resonant Tunneling MESFET" shown schematically in Fig. 2. The channel width a, gate length L, and gate width perpendicular to the plane of Fig. 2, were taken to be 0.20, 0.75, and 20 μm, respectively. The doping in the channel N_D was 1×10^{17} cm^{-3}. The source length d and width, were taken to be 3 and 20 μm, respectively. The device was assumed to be symmetric with respect to the x-axis (Fig. 2).

the channel N_D was 1×10^{17} cm^{-3}. The source length d and width, perpendicular to the plane of Fig. 2, were taken to be 3 and 20 μm, respectively. These curves display the substantial variations of the source–drain $I_D - V_D$ characteristics which may be obtained by modulating the gate voltage. As the latter is decreased, the channel resistance increases, resulting in shifting the positions of the resonances towards larger drain voltages and eventually reducing their peak to valley ratios. For proper operation, the FET must operate in its linear regime. Furthermore, the channel resistance must be smaller than the absolute value of the tunnel structure negative differential resistances over a reasonably wide range of gate bias voltages. Since typical transit times for tunneling through double-barrier heterostructures are on the order of 1 ps or less, the millimeter-wave performance of these devices is limited by the transit time of electrons in the channel. This delay time can be minimized by reducing the gate and channel lengths and by increasing the doping in the channel. Since the minimum gate length in GaAs FET's is about 0.1 μm, the expected maximum frequencies of operation should be on the order of 100 GHz [15]. Because they affect the ultimate performance of the device, the source–gate and gate–drain spacings are key parameters. The best values realized so far are 0.1 and 0.2 μm, respectively [12]. It should also be mentioned that charging times are important in all tunnel structures. We are currently investigating their influence on the speed performance of the proposed devices.

The second proposed device is schematically illustrated in Fig. 4. It consists of a resonant tunneling heterostructure integrated with a vertical MESFET [16]. The source contact is made to the top n^+-GaAs layer. It is followed first by the tunnel structure, and then by the GaAs active channel. Motion of the electrons in the channel is controlled by a Schottky barrier gate. The n^+-substrate acts as the drain. It should be noted that the device could also operate in a configuration in which the source and drain electrodes are interchanged. This structure has several advantages over the first proposed device: (i) the geometry is such that the path of the electrons remains perpendicular to the tunnel barriers; (ii) the fabrication procedure is easier; (iii) the length of the active channel can be further reduced; and (iv) more accurate control of the drain to source spacing can be achieved. This should result in maximum frequencies of operation substantially greater than those obtainable with the previous device configuration.

The third proposed structure, schematically illustrated in Fig. 5, is a resonant tunneling heterostructure integrated with a permeable base transistor (PBT) [17], [18]. After tunneling through the double-barrier heterostructure, the flow of electrons is controlled by a thin metal grating which is embedded within the GaAs and forms a Schottky barrier gate. As in the previous device, the roles of the source and drain can be interchanged. It has been claimed that permeable base devices could, in principle, be capable of achieving maximum frequencies of oscillation near 1 THz [17]. This makes them promising for modulating tunnel structure negative differential resistances. Although it has been difficult in the past to achieve high quality epitaxial growth over metal films, improved growth techniques, or different approaches such as replacing the metal grating by p-type semiconductor grid fingers, appear to be promising.

In summary, we have proposed and analyzed three-terminal devices consisting of resonant-tunneling double-barrier heterostructures integrated with microwave field-effect transistor configurations. The three proposed devices, shown in Figs. 2, 4, and 5, could be called a "Resonant Tunneling MESFET," a "Resonant Tunneling Vertical FET," and a "Resonant Tunneling PBT," respectively. Simulations of device characteristics showed that substantial modulation of the tunnel structure negative differential resistances can be obtained by applying a gate voltage. Because they could operate in microwave and millimeter-wave regimes, such three-terminal devices should find applications in high-speed digital circuits, tunable millimeter-wave oscillators, and negative resistance amplifiers. Although these devices were presented in the context of GaAs/Al$_x$Ga$_{1-x}$As heterojunction technology, they could be implemented in other materials. It may actually be advantageous to use semiconductors such as InGaAs, which has a higher electron mobility than GaAs. Experimental

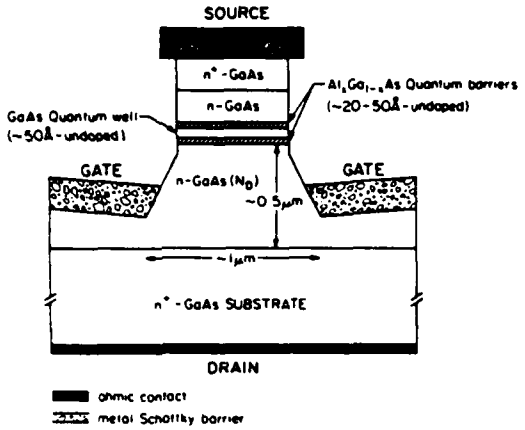

Fig. 4. Schematic diagram (not to scale) of a cross section of the second proposed transistor structure, the "Resonant Tunneling Vertical FET."

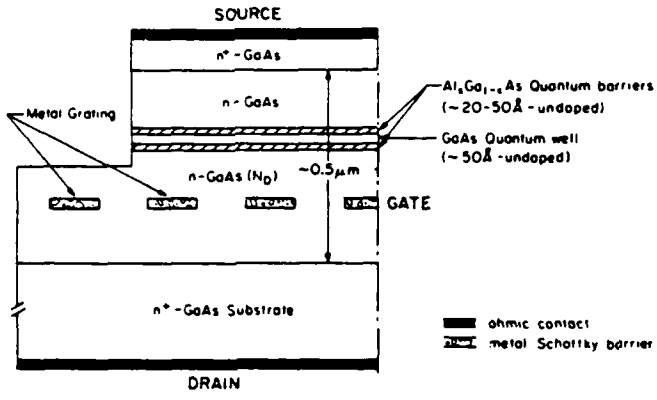

Fig. 5. Schematic diagram (not to scale) of a cross section of the third proposed transistor structure, the "Resonant Tunneling PBT."

investigations are under way to determine the properties of these structures and to explore their possible applications in high-frequency analog and digital circuits.

Acknowledgment

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Schottky barrier height measurements of epitaxial $NiSi_2$ on Si

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Photoresponse measurements of the Schottky barrier heights of epitaxial $NiSi_2$ layers on nondegenerate n-(111) Si, for type-A and type-B orientations, have been performed. The type-A and type-B cases are consistently observed to differ in barrier height by greater than 0.1 eV. We obtain measured values for ϕ_{B_0} (at $T = 300$ K) of 0.62 ± 0.01 eV and 0.77 ± 0.05 eV for type A and B, respectively.

Recently, there has been interest in high quality, molecular beam epitaxially (MBE) grown silicide/Si interfaces because of the potential for studying Schottky barrier formation mechanisms for the first time on a well-characterized epitaxial metal-on-Si system. In particular, a controversy has emerged over the dependence of Schottky barrier height on the microstructure near the $NiSi_2$/Si interface.[1,2] $NiSi_2$ can grow epitaxially on a (111) Si surface in one of two possible orientations, designated type A and B. (Type A is aligned exactly with the substrate and type B differs by a 180° rotation about the substrate normal.) It has been reported by Tung[1] that there is a correlation between silicide orientation and the Schottky barrier height for the case of $NiSi_2$/Si structures. In particular, it is reported that type-A epitaxy results in a barrier height (ϕ_{B_n}) of 0.65 eV, whereas a significantly greater barrier height (0.79 eV) is observed for type B. On the other hand, Liehr, Schmid, LeGoues, and Ho[2] also observe high and low barrier heights but attribute their results instead to the degree of epitaxial perfection at the $NiSi_2$/Si interface rather than the epitaxial orientation.

It is clear that understanding the dependence of observed Schottky barrier heights on such considerations is essential to a basic understanding of the metal-semiconductor interface. At present, there are two distinct explanations[1,2] for the observed difference (>0.1 eV) of barrier heights of $NiSi_2$/Si systems. Since the role that processing details play in the attainment of high quality structures is not completely known, it is useful to introduce an independent set of barrier height measurements made on samples with fabrication details which differ from those previously reported. In this letter we present photoresponse measurements of Schottky barrier heights obtained for type-A and type-B $NiSi_2$/Si samples, measured at $T = 300$ K. The photoresponse technique shows a clear difference between the two orientations, and we believe that it will prove useful in resolving the current controversy. We find values for the type-A and type-B barrier heights in good agreement with the results reported by Tung.[1] However, the photoresponse measurements on type-B samples show deviation from ideal behavior at photon energies close to and below the nominal Schottky barrier.

The samples used in this study were fabricated by molecular beam epitaxial (MBE) techniques in a VG Semicon, Ltd. silicon MBE system. Prior to Ni deposition, the Si substrates were sputter cleaned and annealed (850 °C) in the UHV system. After the anneal, the wafers showed a high quality 7×7 reflection high-energy electron diffraction (RHEED) pattern with no indication of SiC spots.[3] The chemical cleaning technique (Ishizaka *et al.*[4]) followed by thermal evaporation of the oxide in the UHV system as used by Tung[1] was not used in this study. Template layers of type-A and type-B $NiSi_2$ were formed by e-beam evaporation of Ni with subsequent annealing steps, following the procedure of Tung.[5] Type-A and type-B structures thicker than 70 Å were formed either by deposition of pure Ni or co-deposition of Ni and Si onto the appropriate template layer at 650 °C. A total of three type-A and four type-B samples was grown with thicknesses ranging from 70 to 600 Å. Cross-sectional transmission electron microscopy (TEM) studies of a 250-Å thick type-A sample and a 600-Å-thick type-B sample showed very uniform, high quality $NiSi_2$ films entirely of one orientation. In addition, channeling measurements on these two samples showed good channeling minimum yields ($\chi_{min} < 4\%$), and indicated that each sample was predominantly of a single orientation. Further details on the growth conditions and structural characterization of all samples will be published elsewhere.[6]

Photoresponse measurements were made on broad-area-coverage portions of the type-A and type-B wafers. The wafers were cleaved into ~3-mm triangular pieces and then mounted with a drop of silver paint, silicide down, on a transistor header. Care was taken not to puncture the silicide layers. The silver paint mount constituted the device front contact; the back contact was achieved by Al wire bonding to the back side at suitable points. (The back contact is not a good ohmic contact, but this fact did not affect the measurement discussed below because the contact impedance was always much less than the 100-MΩ input impedance of the lock-in amplifier.) The I-V characteristics were checked using a curve tracer. No appreciable leakage currents aside from the normal reverse currents of the $NiSi_2$/Si diodes were observed in each instance, and all reverse characteristics showed strong light sensitivity. The open-circuit photovoltage was then measured as a function of photon energy. Light from a tungsten-filament lamp was directed through a SPEX model 1269 spectrometer, chopped at 270 Hz, and focused with the use of a microscope objective lens onto a small (~0.1-mm-diam) spot on the Si side of the sample, avoiding illumination of the wire-bond contacts (though in practice this last precaution did not seem to affect the results). A long-wavelength pass filter was used to prevent above-band-gap light from illuminating the sample. The

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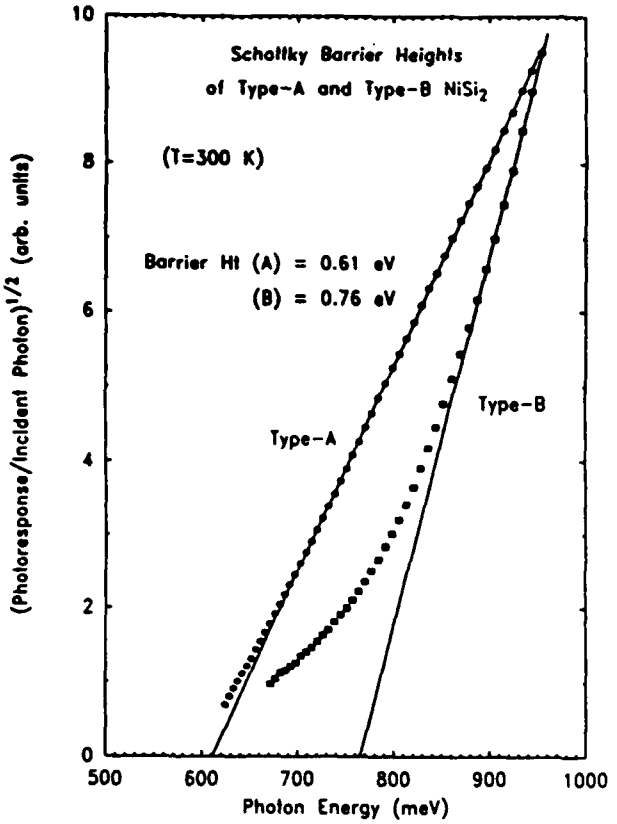

FIG. 1. Photoresponse data for $NiSi_2$/Si samples, for both type-A and type-B orientations. For clarity, data points are displayed only once every 28 actual data points. The barrier heights for type-A (250 Å) and type-B (600 Å) samples are (with image force correction) $\phi_{B_0} = 0.62 \pm 0.01$ and 0.77 ± 0.05 eV, respectively.

photoinduced voltage signal was measured with a PAR model 124A lock-in amplifier, digitized, and stored on a Nicolet model 1170 signal averager. Completed scans could be down loaded to a VAX-11/785 computer for analysis. The optical system response was measured with the aid of a Molectron model P4-42 pyroelectric detector.

The results of the photoresponse measurements at $T = 300$ K are presented in Fig. 1 for selected type-A and type-B samples and are typical of the samples used in this study. In this figure we plot the square root of the photovoltage per incident photon as a function of photon energy. Extrapolation of the curve to the photon energy axis yields directly[7] the effective barrier height ϕ_{B_e}. (This differs from the intrinsic barrier height ϕ_{B_0} by the image force lowering, which for the present samples with a phosphorus doping level of $\sim 1.5 \times 10^{15}$ cm^{-3}, is about 12 meV for the type-A and 14 meV for the type-B samples.) The results give a value for the type-A interface of $\phi_{B_0} = 0.62 \pm 0.01$ eV, with the image force correction. This barrier height was obtained for all three type-A samples whose thicknesses range between 250 and 600 Å. Forward *I-V* measurements that we have made as a check on this result yield a value of $\phi_{B_0} \approx 0.63$ eV with ideality factors near 1.04. These *I-V* measurements were made on four black wax-defined $NiSi_2$ mesas roughly 200–1000 μm in diameter on a type-A sample with an ohmic back contact. Our results for the type-A samples are in fair agreement with the value reported by Tung,[1] but are in disagreement with values reported by Liehr *et al.*[2] for the case of good type-A epitaxy. We point out that some of our fabrication procedures, particularly the substrate precleaning step, are different from those employed by either of these workers. All of our microstructure studies indicate the samples to be very high quality epitaxy with little interfacial disorder.

The type-B result is less straightforward. From Fig. 1 we see that the data for this case do not contain a clear linear portion as do the type-A data. If we extrapolate the high-energy portion of the curve we obtain a barrier height of 0.77 ± 0.05 eV, where the uncertainty was estimated by considering the effect of varying the fit range on the position of the intercept. However, forward *I-V* measurements for this case yield a value around 0.70 eV with a high ideality factor (~ 1.10). The unusual features of the type-B photoresponse data may be related to the observation of a prominent interface peak which can be seen in channeling data from the 600-Å-thick $NiSi_2$ sample, which otherwise shows a good minimum yield ($\chi_{min} \approx 3.8\%$). No such interface peak was observed in channeling data for type A. We note here that the type-B results shown in the figure are typical of all four type-B samples, including the sample with a $NiSi_2$ layer thickness of 70 Å. Our type-B barrier height measured by photoresponse at high photon energies is in excellent agreement with Tung's reported type-B barrier height[1] of 0.79 eV. However, the presence of regions of interfacial imperfection may tend to lower the barrier height observed by the electrical measurement, and complicate the shape of the photoresponse curve at lower photon energies. In any case, the photoresponse for type-B $NiSi_2$ is clearly different and shows a larger ϕ_{B_0} than for type-A; this is in qualitative agreement with Tung's results.

In summary, we have measured using photoresponse the barrier heights of high quality, single crystal type-A and type-B $NiSi_2$/Si structures. We obtain values of the intrinsic barrier height (ϕ_{B_0}) of 0.62 ± 0.01 eV and 0.77 ± 0.05 eV for the case of type-A and type-B epitaxy, respectively. We find that, for our high quality type-A samples that we confirm the results of Tung but disagree with the results reported by Liehr *et al.* For the case of type-B epitaxy, we note that the barrier height observed here is substantially greater (> 0.1 eV) than that of type A, again in agreement with Tung's results. It appears, however, that the unusual shape of the photoresponse curve for this case may be the result of the presence of small regions which have a *lower* barrier height than the proper type-B value.

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Schottky barrier height measurements of type-A and type-B $NiSi_2$ epilayers on Si

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Schottky barrier heights of single-crystal type-A and type-B $NiSi_2$ epilayers on nondegenerate *n*-(111) Si have been measured by photoresponse and forward *I–V* methods. High-quality molecular beam epitaxy grown $NiSi_2$ layers of thicknesses ranging from 70 to 600 Å on sputter-cleaned, P-doped Si subtrates ($\sim 1.5\times 10^{15}$ cm^{-3}) were studied. The type-A and type-B orientations consistently yield photoresponse barrier heights which differ by greater than 0.1 eV. We observe the value $\phi_{B_n} = 0.62 \pm 0.01$ eV for all type-A structures from both photoresponse and *I–V* measurements. However, we obtain a discrepancy between barrier heights measured by *I–V* ($\phi_{B_n} = 0.69 \pm 0.01$ eV) and photoresponse ($\phi_{B_n} = 0.77 \pm 0.05$ eV) methods, and in addition consistently observe an unusual bowing of the type-B photoresponse curves at low photon energies. We show that both the detailed shape of the type-B photoresponse curves and the discrepancy between *I–V* and photoresponse-measured barrier heights can be accounted for by modeling the type-B barrier as a mixture of high and low barrier regions. Quantitative agreement with experiment is obtained for the values $\phi_{b_1} = 0.81 \pm 0.01$ eV and $\phi_{b_2} 0.64 \pm 0.01$ eV, with effective fractional area coverages of 91% and 9% for high- and low-barrier regions, respectively.

I. INTRODUCTION

Recently, there has been much interest in single-crystal $NiSi_2$ thin films grown epitaxially on Si by molecular beam epitaxy (MBE).[1–4] $NiSi_2$ is one of the few known metallic silicides which closely lattice-matches Si ($<0.4\%$) and can be grown by MBE to form a nearly ideal metal/semiconductor interface.[1–4] $NiSi_2$ is also unique in that single-crystal silicide layers can be fabricated on (111)-Si in two distinct orientations with respect to the Si substrate, designated type A and type B.[1] (Type-A layers are aligned exactly with the Si lattice while type-B differs by a 180° rotation about the substrate normal.) Hence, MBE-grown $NiSi_2$/Si interfaces provide us for the first time with a high-quality, well-characterized structure for advancing our understanding of Schottky barrier formation, and as such have been the subject of active investigation.[1–4]

At present, a controversy exists over the observed difference (greater than 0.1 eV) in Schottky barrier heights (SBH) of high quality MBE-grown $NiSi_2$/*n*-(111) Si systems: On the one hand, it has been reported by Tung[2] that the SBH depends on the *orientation* of the silicide epilayer, while on the other hand, it has been reported by Liehr *et al.*[3] that the SBH is independent of epitaxial orientation but instead depends on the *structural perfection* of the $NiSi_2$/Si interface. Should the SBH prove to depend on silicide orientation, the result would have major implications for theories of Schottky barrier formation,[5–7] which at present do not account for this phenomenon at a fundamental level. Even if the SBH should prove to be independent of silicide orientation, it is still of considerable practical interest to identify the origin of the reported difference in SBH results. In both studies[2,3] channeling and TEM measurements suggested high quality single-crystal $NiSi_2$ layers of either type-A or type-B orientation. However, these characterizations are not always sensitive to aspects of the *interface* region which can have a profound effect on the electrical behavior. It is therefore important to examine an independent set of SBH measurements made on samples whose fabrication details differ from those of Tung[2] and Liehr *et al.*[3] The main difference between our work and that of Tung and Liehr *et al.* was the substrate surface cleaning technique used. In our work, sputter cleaning followed by an 850 °C anneal was employed, in contrast to the higher temperature thermal cleaning methods used by Tung[2] and Liehr *et al.*[3]

In previous work[4] we have reported the observation of an orientation dependence of the SBH. We found that our SBH's as determined by photoresponse were essentially in agreement with those of Tung[2] as measured by *I–V* and *C–V* methods although several features of our type-B results went unresolved; in particular, the unusual shape (and hence, difficult interpretation) of the Fowler plot, and a 0.08 eV discrepancy between photoresponse and *I–V* determined SBH. In this paper we reexamine our previous photoresponse results, and supplement them with more extensive *I–V* measurements. For type-A structures, both methods are found to consistently yield a SBH of $\phi_{B_n} = 0.62 \pm 0.01$ eV. For type-B samples we always observe a SBH of 0.69 ± 0.01 eV from *I–V* measurements, and consistently see a "bowing" of the Fowler plot which was previously interpreted as corresponding to a barrier height of $\sim 0.77 \pm 0.05$ eV, where the uncertainty was mainly associated with interpretation rather than reproducibility of the result. We will show below that both the detailed shape of the Fowler plot *and* the measured *I–V* SBH can be *quantitatively* accounted for by modeling the type-B structure as an electrically parallel combination of regions of high and low barrier height.

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II. EXPERIMENTAL

A. Silicide fabrication and structural characterization

The experimental details pertinent to this work have already been discussed in detail in Ref. 4 and the reference therein, so here we limit ourselves to a brief mention of sample fabrication and characterization. In this study, type-A and type-B single-crystal $NiSi_2$ films ranging in thickness from 70–600 Å were grown by e-beam evaporation either of pure Ni or by coevaporation of Ni and Si onto type-A or type-B template layer at 650 °C. The template layers were formed following the methods developed by Tung[1,8] and annealed at 500 °C. In contrast with Tung[2] and Liehr *et al.*,[3] the Si substrates used in our work ($\sim 1.5\times 10^{15}$ cm^{-3},P-doped) were sputter cleaned with subsequent annealing at 850 °C. Both the cleaning and film deposition steps took place in a single UHV chamber (base pressure $\sim 2\times 10^{-11}$ Torr). The resulting $NiSi_2$ films have been extensively characterized by high-energy ion channeling, TEM, and x-ray diffraction, and show both the type-A and type-B structures to be of high quality.[9]

B. Electrical characterization

Photoresponse and forward I–V methods were used to measure the SBH of the type-A and type-B samples. The photoresponse measurements were performed by the backillumination method[10] on broad area $NiSi_2$ layers, with the use of a calibrated spectrometer. The open-circuit photovoltage was synchronously detected at levels such that $V_{ph} \ll kT$, insuring the linearity of the voltage response. The I–V measurements were made on lithographically defined devices varying between 360–1300 μm in diameter. A Au-wire probe directly on the silicide was used as the device contact in the I–V measurements presented here although it was observed that wire-bonding directly to even the thinnest (70 Å) $NiSi_2$ layers resulted in only a slight increase in leakage current. Series resistance due to the high bulk substrate resistivities necessitated numerical correction to the raw I–V characteristics, following Norde.[11] All SBH measurements were performed at room temperature.

III. RESULTS AND DISCUSSION

A. Photoresponse measurements of SBH

The results of the photoresponse measurements of SBH from our previous work[4] are summarized in Fig. 1. In this figure we present response curves taken at $T = 300$ K for typical type-A and type-B samples plotted according to the conventional Fowler analysis.[10,12] In the conventional analysis the resulting curve should contain a linear region for $(\hbar\omega - \phi_{B_n}) > 3$ kT, where $\hbar\omega$ is the photon energy, which, when extrapolated to the abscissa, gives the barrier height ϕ_{B_n} directly. As shown in Fig. 1, the type-A data can be clearly extrapolated to an intercept value of 0.61 eV. Applying an "apparent barrier height" correction (difference between ϕ_{B_n} and the extrapolated value) as discussed by Okumura and Tu,[13] we finally obtain for the type-A SBH, the value of 0.62 eV. This value is reproduced within 0.01 eV on all of our type-A samples. Turning now to the type-B

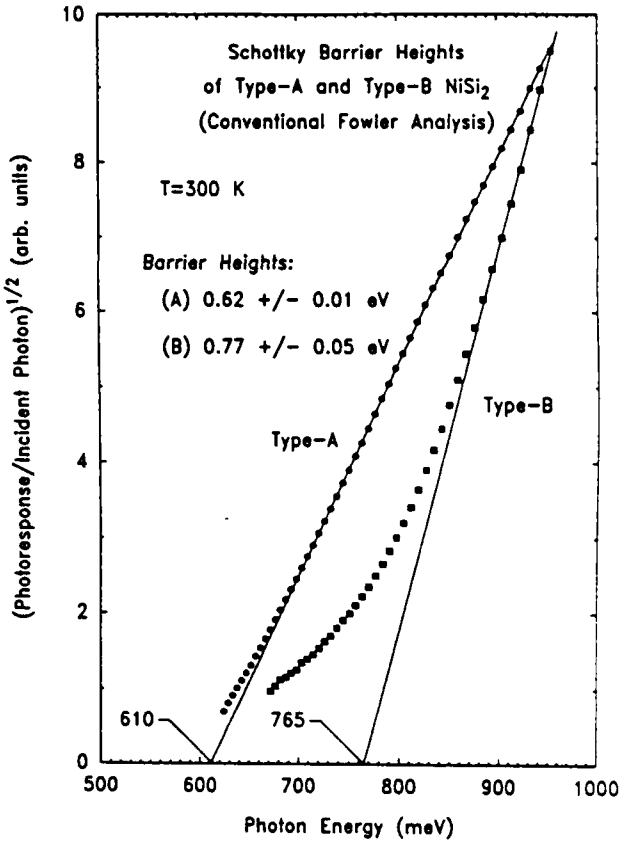

FIG. 1. Photoresponse data for $NiSi_2$/Si samples, for both type-A and type-B orientations. For clarity, data points are displayed only once every 28 actual data points. The barrier heights for type-A (250 Å) and type-B (600 Å) samples are (with apparent barrier height correction) $\phi_{B_n} = 0.62 \pm 0.01$ and 0.77 ± 0.05 eV, respectively.

photoresponse, we see from the figure that the data do not contain a clearly linear region, making conventional SBH interpretation difficult. In our previous work[4] we suggested that our type-B interfaces may contain local regions of lower SBH, resulting in the observed bowing effect in the curve at decreasing photon energies. Despite their unusual shape, our type-B photoresponse curves are quite reproducible over the full range of $NiSi_2$ layer thicknesses from 600 down to 70 Å, where one would expect the best pseudomorphic growth. Previously,[4] we have extrapolated from the upper part of the type-B curve to a SBH of 0.77 eV and quoted a rather large uncertainty (0.05 eV).

B. I–V measurement of SBH

For comparison we have made careful forward I–V measurements of the SBH for type-A and type-B structures. These results are summarized in Fig. 2. As shown in the figure, we obtain a clear difference between type-A and type-B epitaxy. In most cases, the results (after applying a series resistance correction) are reproducible from device to device and from sample to sample within 0.01 eV, the only complication arising from samples with nonlinear back contacts, which were excluded from consideration. The excellent reproducibility of SBH and linearity over two or more

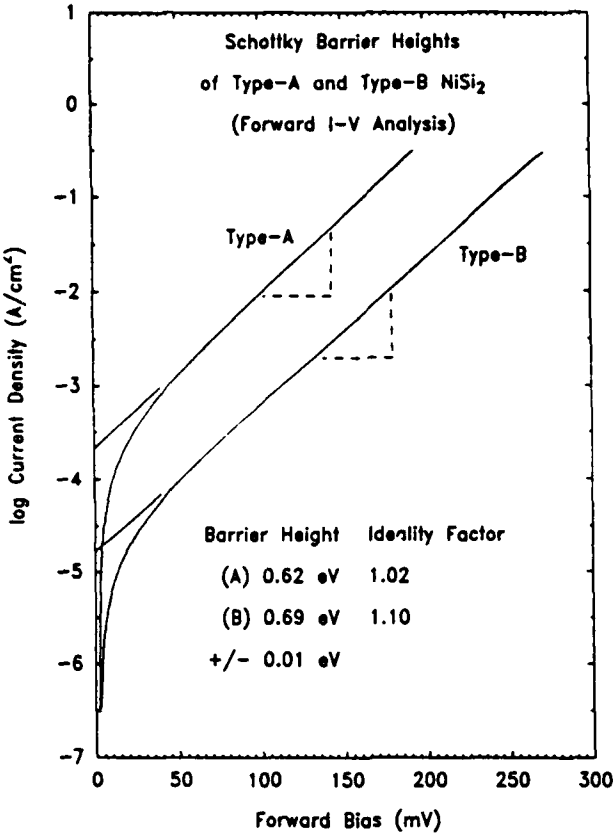

FIG. 2. Forward I–V measurements, corrected for series resistance, of Schottky barrier height for type-A and type-B $NiSi_2$/Si samples, taken at $T = 300$ K. The type-A and type-B barrier heights are 0.62 and 0.69 $\pm$ 0.01 eV with ideality factors of 1.02 $\pm$ 0.02 and 1.10 $\pm$ 0.01, respectively. A value of 110 A/cm^2 K^2 was used for the effective Richardson constant.

decades of log J vs V demonstrates the adequacy of our procedures. For type-A layers we obtain $\phi_{B_n} = 0.62$ eV with typical ideality factors $\eta = 1.02 \pm 0.02$, and for type-B we find $\phi_{B_n} = 0.69$ eV with $\eta = 1.10 \pm 0.01$.

C. Double Schottky contact model

It is clear from Figs. 1 and 2 that the type-A SBH measured by photoresponse and I–V methods are in excellent agreement, but that there is a significant discrepancy ($\sim$0.08 eV) for the case of type B. We now show that we can account for both the detailed shape of the type-B photoresponse and the observed numerical value of the I–V SBH measurement in terms of a model for the type-B interface consisting of an electrically parallel mixture of regions of high and low SBH, ϕ_{hi} and ϕ_{lo}. Okumura and Tu[13] have considered the response from compound barrier structures in detail. This analysis is based on the combined photoresponse Y of a parallel set of SBH's $\{\phi_i\}$ being given by

$$Y(\hbar\omega,T;\{\phi_j\}) = \sigma\sum_i \alpha_i C_i F(\hbar\omega,T;\phi_i), \qquad (1)$$

where $F(\hbar\omega,T;\phi_i)$ is a normalized Fowler-type photoyield function,[12] α_i corresponds to the fractional area coverage of barrier ϕ_i, σ is the active device area, and C_i is a factor which depends on the thickness, reflectivity, absorptivity, and electron attenuation length of the appropriate metal layer.[13] In our high/low barrier model we take $C_i = C = \text{const}$ and define a new normalization constant $\sigma' \equiv C\sigma$. Eq. (1) then becomes

$$Y(\hbar\omega,T;\phi_{lo},\phi_{hi}) = \sigma'[\alpha F(\hbar\omega,T;\phi_{lo}) + (1-\alpha)F(\hbar\omega,T;\phi_{hi})], \qquad (2)$$

where α refers to the effective areal fraction covered by ϕ_{lo}.

With the use of the above model we are now in a position to analyze the type-B photoresponse data. Okumura and Tu[13] have developed a general method to analyze mixed Schottky barrier structures which requires differentiation of the photoresponse curve with respect to $\hbar\omega$, which is then analyzed in terms of derivatives of Eqs. (1) or (2). However, in our work we find it both adequate and much simpler to use Eq. (2) directly. Treating the quantities, ϕ_{hi}, ϕ_{lo}, α, and σ' as adjustable parameters, we perform a least-squares fit to our experimental type-B photoresponse data using Eq. (2) evaluated at $T = 300$ K. The result is shown in Fig. 3. We see that good agreement with experiment is obtained for the values, $\phi_{hi} = 0.81$ eV, $\phi_{lo} = 0.64$ eV, $\alpha = 0.09$. We mention here that applying this fit procedure to all of our type-B samples, from 70 to 600 Å film thicknesses, yield consistency in barrier heights of $\pm$ 0.01 eV and in α of $\pm$ 0.02. In princi-

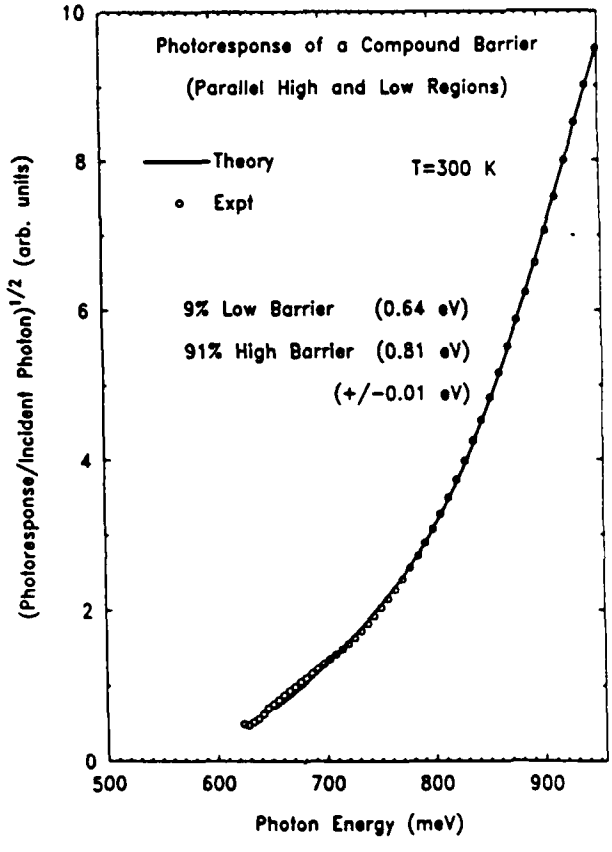

FIG. 3. Least-squares fit of the double Schottky contact model (see text) to type-B photoresponse data, at $T = 300$ K. The fit ranges over 1200 data points, corresponding to energies covered by the solid line. The three physically meaningful fit parameters are the barrier heights $\phi_{hi} = 0.81$ eV, $\phi_{lo} = 0.64$ eV, and low-barrier areal coverage $\alpha = 9\%$.

ple, a double Schottky contact should be directly observable as a "kink" in the first derivative[13] or as a double plateau in the second derivative[14] of the photoresponse curve. However, it is straightforward to demonstrate that, for the present case, the first and second derivative spectra do not themselves yield useful information about the double contact structure at room temperature without again resorting to the type of fit described above.

Next, we use the results of the model fit to account for the observed I–V SBH for type-B samples. For parallel Schottky contacts we can define an average barrier height $\bar{\phi}$ through the expression for Schottky barrier saturation current density[10] as

$$e^{-\bar{\phi}/kT} \equiv \sum_i \alpha_i e^{-\phi_i/kT}. \tag{3}$$

Neglecting appreciable differences in ideality factors for the high- and low-barrier regions, it is the *single* SBH, $\bar{\phi}$, that would be observed in an I–V measurement. It is straightforward to show that, for the present case, Eq. (3) leads to the expression

$$\bar{\phi} \simeq \phi_{lo} - kT \ln \alpha, \tag{4}$$

valid whenever $\alpha \exp[(\phi_{hi} - \phi_{lo})/kT)] \gg 1$. Using the values of ϕ_{hi}, ϕ_{lo}, and α obtained from the model fit above yields $\bar{\phi} = 0.70$ eV, in excellent agreement with the type-B SBH directly measured by the I–V method (0.69 eV). It is easy to show that taking proper account of the ideality factors leads to a correction term in Eq. (4) of $\simeq -qV(\Delta\eta/\bar{\eta}^2)$, where qV is the forward bias (in eV), $\bar{\eta}$ is the mean ideality factor, and $\Delta\eta$ the difference between the low-barrier ideality factor and $\bar{\eta}$. From this we see that neglecting the ideality factors leads to an error of less than 0.01 eV for reasonable values of the ideality factors. Thus, with a simple model we have shown quantitative consistency between apparently disparate SBH results for the case of type-B $NiSi_2$ layers measured by two different methods.

D. Interpretation

The interpretation of our photoresponse and I–V SBH measurements suggest that most (91%) of the interfacial area of our type-B $NiSi_2$/Si structures is associated with a SBH of 0.81 eV, but also present are localized regions, comprising 9% of the effective device area, that are associated with a reduced barrier height, 0.64 eV. There are two possibilities that immediately spring to mind to account for this phenomenon. Noting that the value of ϕ_{lo} is close to the type-A SBH, it may be that simultaneously present at the $NiSi_2$/Si interface are grains of type-A orientation mixed in among the type-B structure. This possibility is discounted by our channeling and TEM observations, however, which show both our type-A and type-B films to be of comparable quality. A second possibility is that localized interfacial structural disorder gives rise to localized electronic states of sufficient density to locally pin the Fermi level. Dislocations are observed[9] in plane view TEM images of type-B $NiSi_2$ while none are observed in type-A films over the range of thickness reported here. However, since the density of dislocations increases with increasing type-B film thickness, the consistent observation of bowing in the photoresponse for all type-B layers argues against misfit dislocations as the cause. It is possible that the low barrier height regions may be associated with the localized *planar* defects seen in high resolution TEM, as discussed in Ref. 9. At the present time the case of these planar defects is not understood and is under investigation. Finally, the absence of any nonideality in the physical or electrical characterization of the type-A structures and the significant difference between type-A and type-B measured barrier heights would suggest the absence of some foreign surface contaminant which dominates the electrical behavior near the interface.

IV. SUMMARY

In summary, we have made Schottky barrier height measurements on high-quality, MBE-grown $NiSi_2$/Si structures of type-A and type-B orientations with the use of photoresponse and forward I–V techniques. Comparison of the data obtained from both techniques clearly demonstrate a difference in barrier heights between type-A and type-B structures. This finding is in agreement with the results of Tung[2] but in disagreement with the results of Liehr *et al.*[3] The main contribution from this paper is the side-by-side comparison of photoresponse and I–V measurements made on the *same* samples, and the unique comparison that these complementary measurements allow. For the case of type-A epitaxy, we consistently obtain a barrier height from both techniques of $\phi_{B_n} = 0.62 \pm 0.01$ eV. For the case of type-B, a serious discrepancy in the barrier height between photoresponse and forward I–V methods is observed. Furthermore, the qualitative shape of the type-B Fowler plots are nonlinear but consistent from sample to sample, rendering determination of barrier height ambiguous. We have shown that both the detailed shape of the Fowler plot as well as the measured I–V value of type-B barrier height for our samples can be quantitatively accounted for in terms of a double Schottky contact model. In this model, the type-B structure consists of electrically parallel regions of high and low barrier height, where $\phi_{hi} = 0.81 \pm 0.01$ eV, $\phi_{lo} = 0.64 \pm 0.01$ eV, with the effective area of low- and high-barrier coverages being 9% and 91%, respectively. The possible physical realizations of this model within the $NiSi_2$/Si system are discussed.

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Summary Abstract: Schottky barrier height measurements of type A and type B $NiSi_2$ on Si

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The Schottky barrier heights of high quality MBE-grown $NiSi_2$ epi-layers on Si have been measured by photoresponse and forward I–V methods. $NiSi_2$ is one of the few known metallic silicides which lattice matches Si and can be grown by molecular beam epitaxy (MBE) to form a nearly ideal epitaxial metal-on-semiconductor system.[1-4] $NiSi_2$ is also unique in that it can be grown epitaxially on (111) Si in two distinct orientations, designated type A and type B, with respect to the Si substrate.[1] For these reasons $NiSi_2$/Si interfaces provide a novel, well-characterized structure for the study of Schottky barrier formation, and have recently been the subject of active investigation.[1-4] At present, a controversy exists over the observed difference (greater than 0.1 eV) in Schottky barrier heights of $NiSi_2$/Si systems: On the one hand, it has been reported by Tung[2] that the barrier height depends on the *orientation* of the silicide epi-layer, while on the other hand, it has been reported by Liehr *et al.*[3] that the barrier height is independent of epitaxial orientation but instead depends on the *structural perfection* of the $NiSi_2$/Si interface. Identification of the correct dependence will have major implications for theories of Schottky barrier formation.

We have made photoresponse measurements of the Schottky barrier heights of epitaxial $NiSi_2$ on non-degenerate n-(111) Si substrates, for the cases of type A and type B epitaxy, on several samples with $NiSi_2$ layer thicknesses ranging from 70 to 600 Å. Nominal doping in all Si substrates was about 1.5×10^{15} cm^{-3}. The photoresponse measurements were performed on broad-area-coverage regions of $NiSi_2$ on Si. No processing subsequent to growth took place on these silicide layers. Samples were illuminated from the back side (i.e., through the Si substrate) with the use of a calibrated monochromatic light source, and the open-circuit photovoltage was measured as described in Ref. 4. The crystalline quality of our type A and type B silicide layers was verified by cross-sectional transmission electron microscopy (TEM) and ion-channeling measurements, although a prominent interface peak was observed in channeling data on type B samples.[5] We consistently observe a difference in Schottky barrier height greater than 0.1 eV between type A and type B structures. At $T = 300$ K we obtain the values $\phi_{Bn} = 0.62 \pm 0.01$ eV and 0.77 ± 0.05 eV for the barrier heights of type A and type B $NiSi_2$, respectively, from photoresponse measurements, where an apparent barrier height correction[6] of 0.01 eV has been added to the values obtained from the conventional Fowler analysis.[7] The photoresponse curves for all type A samples exhibit linear behavior on a Fowler plot. However, photoresponse curves for all type B samples show a nearly identical deviation from the expected linear behavior at photon energies close to and below the nominal type B Schottky barrier reported by Tung.[2]

In addition to photoresponse, forward I–V methods have also been used in the present work to determine barrier heights for type A and type B samples. Mesa structures of diameters ranging from 360 to 1300 μm were formed by a black-wax mask and etch procedure ($3HNO_3$:$1CH_3COOH$:0.4HF). Ohmic back contacts were obtained by painting an In–Ga amalgam on the back of the sample, though in some cases some nonlinearity in I–V due to the back contact was observed and such samples were excluded from further consideration. A thin Au-wire probe against the silicide layer constituted the device contact. The I–V measurements performed at $T = 300$ K yield barrier heights of $\phi_{Bn} = 0.62 \pm 0.01$ eV for type A samples in excellent agreement with the photoresponse result, with ideality factors $\eta = 1.02 \pm 0.02$. However, for type B we obtain $\phi_{Bn} = 0.69 \pm 0.01$ eV, which is considerably less than the photoresponse value (0.77 eV).

A possible explanation for both the unusual shape of the type B photoresponse curve *and* the discrepancy between electrically and optically obtained values for the barrier height is the presence of interfacial regions of mixed barrier height.[6] We have modeled our type B samples as consisting of an electrically parallel combination of regions of high and low Schottky barrier height, ϕ_{HI} and ϕ_{LO}, respectively. For this model, the observed photoresponse would be an area-weighted superposition of photoresponse components from the high and low barrier regions,[6] whereas the I–V measurement would yield a *single* mean barrier height[8] $\bar{\phi}$. We have performed a nonlinear least-squares fit of our type B photoresponse data with the use of a pair of Fowler-type functions[9] evaluated at $T = 300$ K. This fit involves three parameters—the two barrier heights (ϕ_{HI} and ϕ_{LO}) and the low-barrier fractional area coverage (α). The results of fitting to a number of type B samples of thicknesses from 70 to 600 Å consistently yields the unique set of values, $\phi_{HI} = 0.81 \pm 0.01$ eV, $\phi_{LO} = 0.64 \pm 0.01$eV, and $\alpha = 0.09 \pm 0.02$ eV. A simple calculation[8] shows that for this choice of barrier heights and coverages a forward I–V measurement would yield a single barrier height $\bar{\phi} = 0.70$ eV, in excellent agreement with the actual observed value (0.69 eV).

In summary, our results directly demonstrate a dependence of Schottky barrier height on *orientation* of the $NiSi_2$ layer for high quality type A and type B epitaxy. We find that

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we confirm the results of Tung[2] but disagree with the results reported by Liehr *et al.*[3] For the case of type B epitaxy, we obtain a photoresponse barrier height from conventional Fowler analysis of $\phi_{Bn} = 0.77 \pm 0.05$ eV which is substantially greater than that of type A ($\phi_{Bn} = 0.62 \pm 0.01$ eV). A discrepancy in the measured type B barrier height between photoresponse and forward I–V methods, and a consistent bowing in our type B photoresponse data, are observed. However, this discrepancy, as well as the detailed shape of the type B photoresponse curve, can be quantitatively accounted for by representing the type B structure as a mixture of interfacial regions of high and low Schottky barrier height.

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PAPER 6

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THERMALLY INDUCED TRANSITION METAL CONTAMINATION OF SILICIDE SCHOTTKY BARRIERS ON SILICON

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ABSTRACT

We discuss the results of deep level transient spectroscopy (DLTS), current-voltage (I-V), and Rutherford backscattering spectrometry (RBS) measurements of nickel, palladium, and platinum silicide barriers on n-type silicon which have been annealed at temperatures from 300–800 °C. Reverse-biased leakage currents increase with increasing annealing temperature in all three cases. However, the degradation is almost negligible for the PtSi samples at temperatures which cause the palladium and nickel silicide barriers to become very leaky. For the nickel samples which were still reasonable barriers, DLTS showed no traps. A very small concentration of traps was detected for the high-temperature palladium samples. Significant concentrations of platinum traps were seen in samples of PtSi on silicon annealed at 700 °C and above.

INTRODUCTION

The application of transition metal silicides in LSI and VLSI semiconductor technology is progressing rapidly today.[1] Many of these transition metals form one or more deep level traps in silicon. Indiffusion of transition metals from the silicide layer into the underlying bulk silicon during annealing stages of the processing could cause difficulties. However, the standard techniques — for example, Rutherford backscattering spectrometry (RBS)[2] — presently used to study silicide-silicon structures cannot provide the sensitivity required to detect the small quantity of transition metal contaminants which can poison the underlying silicon ($\geq 10^{11}$ cm^{-3}). Deep level transient spectroscopy (DLTS)[3] is a technique suited for this application. Its sensitivity is $\sim 10^{-4}$ times the shallow dopant concentration, so it is possible to detect in the interesting concentration range.

Here, we present the results of studies of the degradation of platinum, palladium, and nickel silicides on silicon. RBS was used to check the composition of the silicide. Current-voltage (I-V) measurements determined reverse leakage currents. DLTS measurements were used to characterize deep levels in the depletion region in the underlying silicon for the devices with reasonable leakage currents.

EXPERIMENTAL METHOD

The substrates used to fabricate samples for this study were 7-10 Ωcm n-type (100) silicon wafers from Wacker. Wafers were cleaned and then im-

mediately loaded into an ion-pumped vacuum system, where a thin (~ 500 Å) metal film was electron-beam deposited at a pressure less than 3×10^{-7} Torr. During the evaporation, a portion of each wafer was covered by a mechanical mask with 0.75-mm-diam holes to make diodes for the electrical measurements. The wafers were diced, and pieces with broad-area metal coverage were annealed with diodes in a vacuum furnace at pressures below 10^{-6} Torr at temperatures from 300 to 800 °C. Ohmic contacts to the diodes were made by rubbing In-Ga onto the backs of the substrates. Diodes used for DLTS studies were mounted on headers and wire-bonded. The samples with broad-area silicide coverage were used for the backscattering analysis. Further, in some cases in which DLTS measurements could not be made on the silicide-silicon structure due to the degradation of the Schottky barrier, a corresponding broad-area piece was etched in $3HNO_3$:$1CH_3COOH$:0.4HF to remove a 5–10 μm layer. Gold dots were then evaporated onto the freshly exposed silicon, and these diodes were prepared as above for DLTS measurements.

Standard RBS spectra were generated by using a beam of 2-MeV $^{+}He^{4}$ ions incident on the sample at a few degrees off normal incidence. The detection angle was 170°.

DLTS measurements were made using a Boonton 72BD capacitance meter operating at a frequency of one megahertz. A double-boxcar gating scheme was used to analyze the transients which were produced over the temperature range of ~ 100–320 K. In addition, a 20-MHz bridge was used to analyze faster transients to determine the trap activation energy for comparison to literature values.

RESULTS AND DISCUSSION

RBS spectra were taken for the samples to determine the composition of the thin silicide layer and to check for surface smoothness and interface abruptness. Analysis yields surface silicide compositions consistent with Ni_2Si for 300 °C, NiSi for 400–700 °C, and $NiSi_2$ for 800 °C. Figure 1 shows the results for nickel samples annealed at 600, 700, and 800 °C. The low-energy fall-off of the nickel signal is clearly less abrupt as temperature is increased. This blurring could be due to the interface growing less abrupt, the surface morphology becoming rough, or a combination of the two. Similar spectra for the palladium samples are shown in Fig. 2. RBS indicates that the phase for the 300–800 °C samples is Pd_2Si. Again, we see the palladium signal blurring at its low-energy end. RBS spectra for the various platinum silicide samples have been presented elsewhere.[4] The silicide formed was Pt_2Si for the sample annealed at 300 °C and PtSi for the higher temperature samples. The low-energy fall-off of the Pt signal was abrupt for samples annealed below 800 °C. Significant degradation of the silicide was observed in the sample treated at 800 °C for 180 min.

Reverse-biased leakage currents for nickel, palladium, and platinum silicide Schottky barriers annealed at various temperatures are given in Table 1. The degradation at a given temperature is more severe for palladium than for platinum, and even worse for nickel.

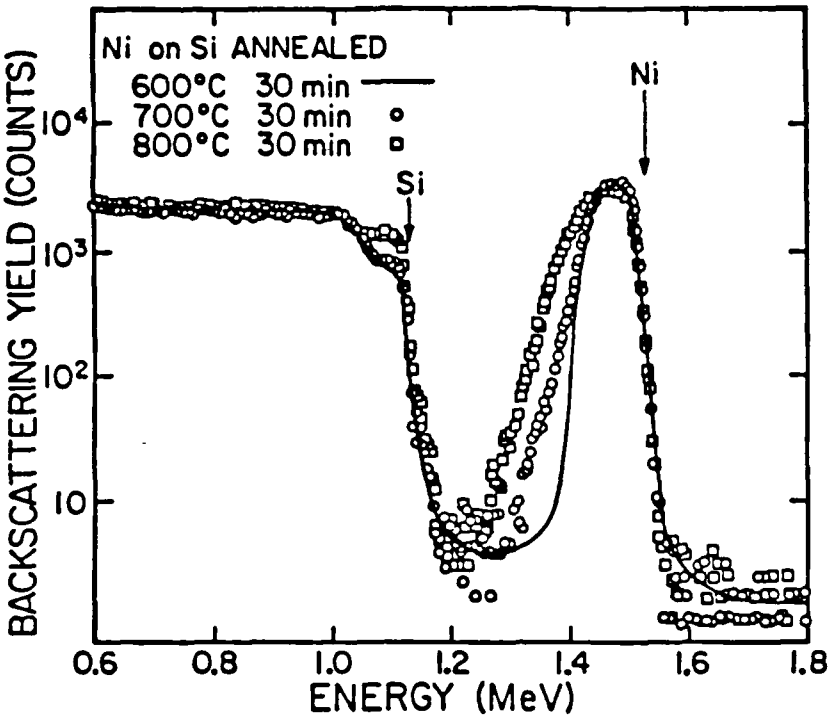

Fig. 1. RBS spectra for nickel-on-silicon structures.

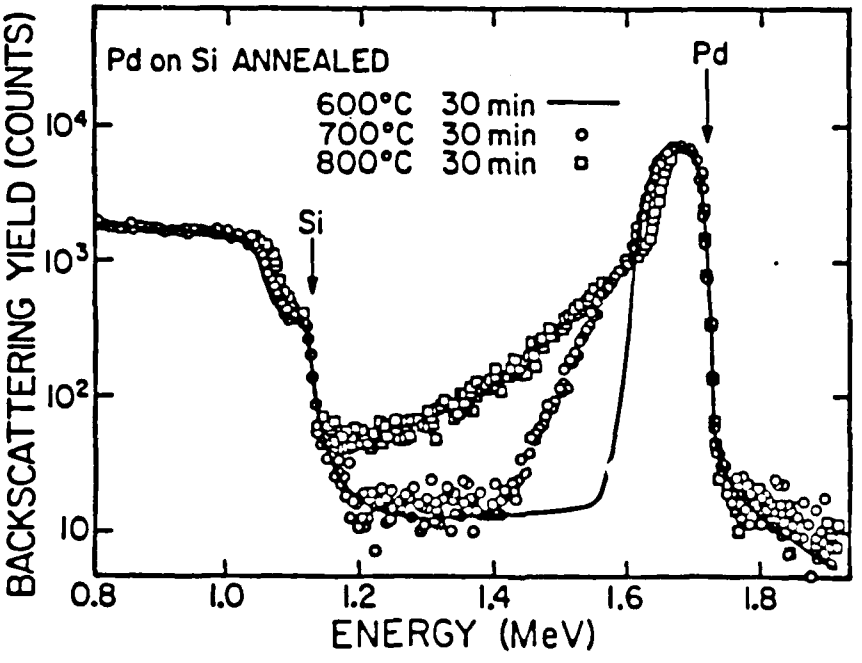

Fig. 2. RBS spectra for palladium-on-silicon structures.

	500 °C	600 °C	700 °C	800 °C
Ni	67 μA	330 μA	2.2 mA	14 mA
Pd	<1 μA	<1 μA	9.1 μA	370 μA
Pt	<1 μA	<1 μA	<1 μA	1 μA

Table 1. Leakage currents at −5 V reverse bias in samples annealed for 30 min.

DLTS spectra were generated with a rate window of 55 s^{-1} for the samples which had sufficiently low reverse leakage currents. The spectra exhibited no traps above a detection limit of $\sim 5\times10^{11}$ traps cm^{-3} in any nickel sample treated below 500 °C. Nickel samples which were treated at temperatures above 500 °C had reverse leakage currents which made DLTS measurements impossible. A piece of nickel material which was annealed at 800 °C was etched and prepared as described above to make DLTS measurements in a region 5–10 μm below the original interface. Again, no traps were detected.

In the case of palladium samples, DLTS spectra exhibited no traps above the detection limit for the samples treated below 700 °C. A barely detectable peak at a temperature of 120 K appeared in the spectrum of the Pd_2Si sample annealed at 700 °C (shown in Fig. 3). Although the signal is so small that it is not possible to make a measurement of the trap activation energy, the location of this peak is consistent with the reported activation energy of 0.22 eV from the conduction band.[5] Thus, we believe that the peak represents a small concentration ($\sim 10^{11}$ cm^{-3}) of palladium electron traps.

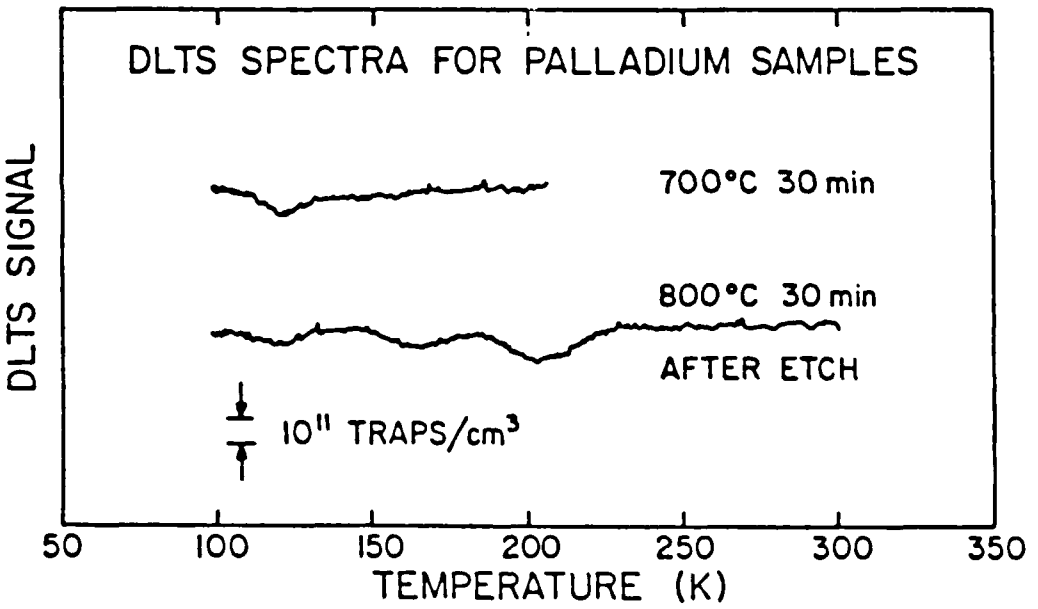

Fig. 3. DLTS spectra of palladium silicide samples taken with boxcar gates at 5 ms and 45 ms for a rate window setting of 55 s^{-1}.

Palladium samples which were treated at temperatures above 700 °C had high reverse leakage currents. As in the case of the high-temperature nickel samples, a piece of 800 °C palladium material was etched to make DLTS measurements below the original interface. The resultant spectrum is shown in Fig. 3. Again, we see a very small peak at 120 K which is probably due to palladium electron traps. In addition, there are minute peaks at 165 and 200 K which were not observed close to the interface in the 700 °C sample. Nor were these peaks seen in the nickel samples which were etched and prepared in exactly the same fashion. These signals may represent the presence of a contaminant (such as iron, a fast diffuser in silicon) which could have been in the palladium charge material used to evaporate the metal onto the silicon substrate. All three peaks correspond to trap concentrations of $\sim 10^{11}$ traps cm^{-3}.

DLTS results for the PtSi samples have been reported in Ref. 4. These samples had very low leakage current even after treatment at 800 °C. No platinum traps were seen in samples annealed below 700 °C, and trap concentrations for the samples treated at temperatures from 700 to 800 °C ranged from $\sim 10^{12}$ to 10^{14} cm^{-3}.

Our RBS studies showed a degradation of the silicide layers for nickel, palladium, and platinum silicides annealed at temperatures above 600 °C. The I-V measurements indicated poor Schottky barrier behavior in nickel samples treated above 500 °C and palladium samples treated above 700 °C. Platinum samples annealed at 800 °C, however, still had reasonable leakage currents. DLTS measurements of the nickel samples with small leakage currents showed no traps. An extremely small number of traps were seen in the 700 and 800 °C palladium samples. Platinum trap concentrations were as high as 10^{14} cm^{-3} in PtSi samples. Thus, we conclude that 700 °C may be regarded as the maximum "safe" temperature at which palladium and platinum silicides may be annealed before transition metal indiffusion begins to degrade the underlying silicon. For our nickel silicide samples, the maximum temperature for good Schottky barrier behavior is only 500 °C.

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PAPER 7

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Tunneling Spectroscopy of Single-Crystal $CoSi_2$ and $NiSi_2$ Epilayers on n-type Si

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ABSTRACT

Electron tunneling spectroscopy experiments have been performed on single-crystal epitaxial silicide films grown on (111)-oriented (off 4°) Si:As. 250 Å-thick films of $CoSi_2$, and type-A and -B $NiSi_2$ on degenerate substrates ($N_d = 2 \times 10^{19}\,cm^{-3}$) have been studied. All spectra show forward bias peaks at energies corresponding to **k**-conserving bulk Si phonons while in reverse bias only the Si TA phonon is observed for $NiSi_2$/Si structures. Plots of dV/dI vs. V for $CoSi_2$/Si structures yield maxima at a forward bias of 39 meV, indicating an enhancement in n-type dopant concentration within $\sim$ 100 Å or more of the silicide-silicon interface.

INTRODUCTION

It has recently become possible to fabricate very high quality, single-crystal films of $CoSi_2$ and $NiSi_2$ on (111)-Si by molecular beam epitaxial (MBE) techniques.[1,2] In addition, it has been demonstrated that single-crystal $NiSi_2$ layers can be fabricated on (111)-Si with comparable quality in either of two distinct orientations (type-A and type-B).[1] A number of interesting device structures based on silicon-silicide heterostructures are being pursued.[3–5] These silicide-on-Si structures are also ideally suited to fundamental studies of metal-semiconductor interfaces, and have been the subject of recent controversy.[6–9]

Electron tunneling transport through the Schottky barrier at a metal-semiconductor interface becomes significant as the depletion length becomes small (< 100 Å). Tunneling effects could become important as transport barriers in devices approach this characteristic size. Through tunneling much can be learned about the factors affecting transport: bulk and defect electronic densities-of-states,[10] dispersion relations of evanescent gap "states",[11] and excitation of elementary processes.[10] In contrast to polycrystalline metal films on Si, there is lattice translational symmetry in the plane of the interface for the case of single-crystal silicides. On this basis it has been suggested[12] that the enhancement of the $\mathbf{k}_{||}$ conservation rule might be manifested in an enhancement in silicide tunneling spectra compared to spectra obtained on polycrystalline films.

In this paper we report the first results of electron tunneling spectroscopy obtained from single-crystal, epitaxial films of $NiSi_2$ (type-A and type-B orientations), and also, of $CoSi_2$ films (type-B orientation), each grown on (111)-Si:As substrates. We obtain similar spectra for both of the silicides studied. Our tunneling spectra contain peaks in forward bias at energies which correspond to **k**-conserving Si phonons. Similar studies on $CoSi_2$ films by Rosencher *et al.*[12] have failed to yield such straightforward spectra. In addition, for $NiSi_2$ films we see a weak antisymmetric peak in reverse bias corresponding to the **k**-conserving Si TA phonon. To the best of our knowledge, our results represent the first observation of **k**-conserving phonons for electron tunneling through a Schottky barrier on n-type Si.

EXPERIMENTAL

Single crystal films of $CoSi_2$ (type-B orientation) and $NiSi_2$ (both type-A and type-B orientation) were fabricated on As-doped Si(111) substrates (off axis by 4°). Nominal substrate doping was determined from Hall and resistivity measurements to be $N_d \approx 2 \times 10^{19}\,cm^{-3}$. Silicide growth took place in an ultrahigh vacuum (UHV), three-chamber Si MBE system (base pressure of 4×10^{-11} mb). Prior to growth, the Si substrates were cleaned either by giving them a modified RCA chemical clean[13] followed by thermal evaporation of the oxide in the UHV chamber, or by sputter cleaning with an Ar ion gun in the MBE system. These cleaning procedures are described in more detail elsewhere[2,9]; we note here, however, that no significant difference in the subsequent results was observed due to the different cleaning methods. The $NiSi_2$ films were grown by using the template techniques established by Tung *et al.*[1] to initiate single crystal growth of type-A or type-B orientations with the final film thickness of 250 Å achieved by codeposition of Si and Ni. Films grown by this technique appear mirror-smooth in Nomarski and have been previously shown to be high-quality, single-crystal films.[9] $CoSi_2$ films were initiated by growing 70 Å of $CoSi_2$ using a pinhole reduction technique[2] and the final thickness of 250 Å was obtained by codepositing Co and Si. In spite of the fact that thinner layers of $CoSi_2$ grown by this technique on lightly doped Si substrates have been of high quality with mirror-smooth surface morphologies,[2] the layers grown for this work showed some texture in Nomarski; the cause of this roughness is not presently understood. However, the films still appear to be high quality, single crystal films as judged by reflection high energy electron diffraction.

Following silicide layer formation and removal from the MBE growth chamber, individual Schottky diode devices were formed. First, a small specimen (suitable for mounting on standard transistor headers) was cleaved from the central portion of the wafer and immersed in 2% HF for approximately 20 sec to remove the native oxide. The specimen was then immediately loaded into a metallization chamber and a Au overlayer ($\approx$ 1000 Å) evaporated. Subsequently, mesa devices ranging from 70 to 700 μm in diameter were defined by conventional photolithographic and wet etch techniques. A commercial etch was used to remove the Au, and then an etch consisting of HNO_3 and HF was used to selectively remove the silicide. Following the etch procedures, the back side of the specimen was scratched with a diamond scribe and an In-Ga amalgam immediately painted on for the ohmic contact (typically 70–90 mΩ at $T = 4.2$ K). The specimen was then mounted with silver paint to a transistor header. Device contacts were made by Al wire-bonding a single lead to the Au overlayer.

Minimum ultrasonic power and bonding time were found necessary to avoid damaging the silicide. The validity of our contacting technique was verified by comparison of zero-bias resistance vs. device diameter data for Al wire-bonded and Au wire-probed devices. When proper care was taken, zero-bias resistances were observed to scale with $(\text{diameter})^{-2}$ at $T = 300$ K and 4.2 K, and the same specific contact resistance for both probed and bonded devices was obtained.

The tunneling spectra (d^2I/dV^2 vs. V) were taken at $T = 4.2$ K with the sample immersed in liquid He. The second derivative signal was directly measured with the use of the standard second-harmonic synchronous detection technique.[10] In addition, direct measurements of dV/dI were made by a similar ac method. The apparatus used for first and second derivative measurements in the present work is described in detail in Ref. 14. Oscillator frequencies of $\omega = 5$ kHz and 50 kHz were used for the first and second derivative measurements, respectively. In addition, a three-point measurement scheme[15] was employed in this study to minimize the effects of the non-negligible series resistance introduced by the back contact.

RESULTS AND DISCUSSION

The results of tunneling spectroscopy experiments performed on $CoSi_2$, and type-A and type-B $NiSi_2$ epitaxial layers on a Si:As substrate are summarized in Fig. 1. In this figure, we present d^2I/dV^2 (the second harmonic signal) as a function of dc bias applied across the tunnel structure. The upper two traces have been vertically displaced from the indicated zero level for clarity. We see that the tunneling spectra obtained from all three types of samples are quite similar in appearance. The strong, antisymmetric structure near $V = 0$ is the so-called zero-bias anomaly[16] and will not be of concern to us here. There are three strong peaks seen in forward bias (electrons tunneling from the Si to the silicide) corresponding to energies of 20, 51 and 60 meV, respectively. In addition, for the $NiSi_2$ samples there is a negative peak of smaller amplitude at a bias of -20 mV. These main features are highly reproducible from sample to sample although some temporal variation has been observed, which we believe to be related to the degradation of our back contacts with time.

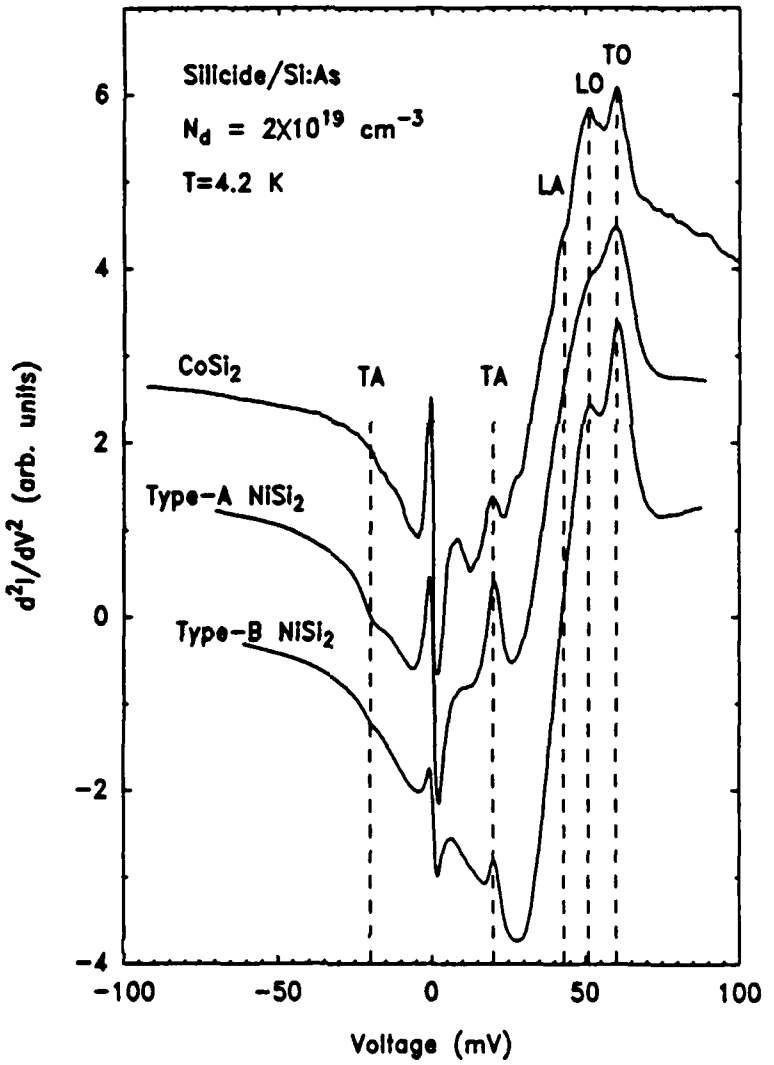

Fig. 1. Second derivative tunneling spectra for $CoSi_2$ and $NiSi_2$ single-crystal films on Si. The principal peaks seen in forward bias correspond to k-conserving bulk Si phonons at energies of 20,51, and 60 ± 1 meV for TA, LO, and TO phonons, respectively. The 43 meV LA phonon position is also indicated. Note the antisymmetric TA peak in reverse bias for $NiSi_2$.

Similar peaks have been reported much earlier on Si Esaki diodes by Chynoweth *et al.*[17] These peaks were identified as **k**-conserving Si bulk phonons. There are a number of similarities between their tunneling spectra and ours: larger peak amplitudes in forward bias, an antisymmetric (TA) peak near $\pm 20\,\mathrm{mV}$, and a barely discernible (LA) peak near $43\,\mathrm{mV}$.[17] In Fig. 1 we see a weak shoulder near the expected LA phonon energy in the $CoSi_2$ tunneling spectrum, but this structure is entirely absent from both of the $NiSi_2$ spectra, and, as we shall see below, is not as reproducible from sample to sample as the larger peaks.

For the Esaki diode, phonon-assisted transport is *necessary* to conserve crystal momentum as the electrons tunnel from the indirect valleys in the *n*-type region into zone-center hole states.[18] However, for the case of metal-semiconductor tunneling, the Fermi surface of the metal is usually large enough in **k**-space to permit unassisted electron tunneling transport to occur.[19] Therefore, it is generally much more difficult to observe **k**-conserving phonons in metal-semiconductor transport. While **k**-conserving phonons have been reported for vacuum-cleaved *n*-Ge/metal systems,[20] we are unaware of any similar results for Si, particularly at the doping levels used in our study. Spectral peaks at the Si LO_Γ phonon frequency ($\approx 65\,\mathrm{meV}$) have been reported for metal films on degenerate *p*-type Si, but in that case, the peaks are *symmetric* with respect to bias direction, and are attributed to modification of the electronic bandstructure due to electron-phonon coupling.[21] In contrast, an *antisymmetric* structure (as observed at $\pm 20\,\mathrm{mV}$ in Fig. 1) indicates (phonon)-assisted inelastic transport.[21]

On this basis we identify the prominent peaks in Fig. 1 with inelastic electron transport assisted by **k**-conserving Si phonons. A virtual electronic state described by an imaginary wave vector connecting the zone-center extrema has been used to theoretically explain the observed bulk phonon structure in *n*-type Ge-metal tunneling spectra.[20] A similar process may account for our results although the direct gap in Si is much larger[18] and the fraction of inelastic tunneling current much weaker.[22] It is worth mentioning here that we evidently do not (unambiguously) see any silicide phonons or final state effects,[10] and the precise significance of the crystallographic perfection of the silicide layer in the observed processes is unclear.

The spectra obtained from $CoSi_2$ samples appear more structured than those from $NiSi_2$. This is shown in more detail in Fig. 2. There, we compare the forward bias portions of scans taken on several devices. We see that, while the major peaks (TA, LO, and TO) reproduce reliably from device to device, there appears to be additional, more complicated structure which does not recur so precisely. We presently do not understand these additional features (which are not seen in the $NiSi_2$ spectra) which may be related to defects or interface states. It is interesting that tunneling spectra for $CoSi_2$/Si:P devices ($N_d = 5 \times 10^{18}\,\mathrm{cm}^{-3}$) reported by Rosencher *et al.*[12]: (1) do not contain our prominent **k**-conserving TA and TO peaks, (2) do contain relatively strong LA and LO peaks in forward bias whereas coupling to longitudinal phonons is much weaker than to transverse phonons for both our devices and for Esaki diodes,[17] and (3) in general appear much more complicated in both bias directions than our Si:As spectra. Points (1) and (3) are consistent with our own unpublished results on Si:Sb substrates of approximately the same doping concentration ($5 \times 10^{18}\,\mathrm{cm}^{-3}$). This suggests that the complicated structure may be related to electron-phonon scattering processes beyond the depletion layer rather than assisted tunneling transport through the Schottky barrier.[23]

Figure 3 shows the results of first derivative measurements dV/dI vs. V. The data were taken on five devices ranging from 70–150 μm in diameter. The figure shows that the specific differential resistance is independent of device size. The zero-bias resistance is $R_0 = (5.7 \pm 0.3) \times 10^{-4}\,\Omega\mathrm{cm}^2$. This value is roughly an order of magnitude smaller

than expected[24] for a doping level of $2 \times 10^{19}\,\mathrm{cm}^{-3}$. The position of the maximum corresponds to a Fermi degeneracy $\mu_F = 39\,\mathrm{meV}$,[25] and hence, a free carrier concentration $n = 3.9 \times 10^{19}\,\mathrm{cm}^{-3}$. Since n is greater than the bulk concentration determined by Hall measurements, we have direct evidence of enhancement of the doping concentration at edge of the depletion layer ($\sim 100\,\text{Å}$ from the interface). Similar evidence for enhancement is observed for type-A and type-B $NiSi_2$. This enhancement is currently under investigation.

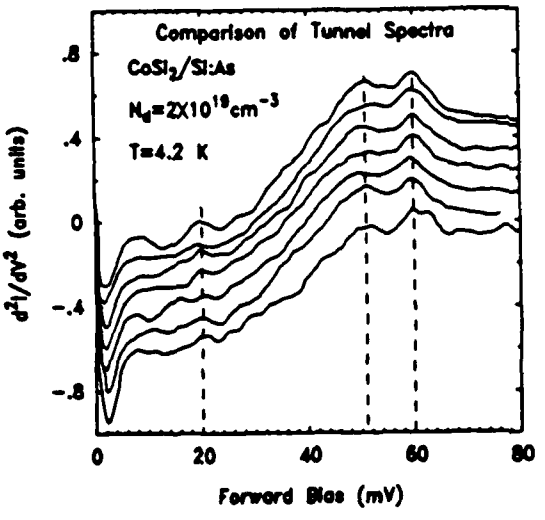

Fig. 2. Tunnel spectra compared for several $CoSi_2$ devices. The three principal peaks (indicated) reproduce well while other features do not.

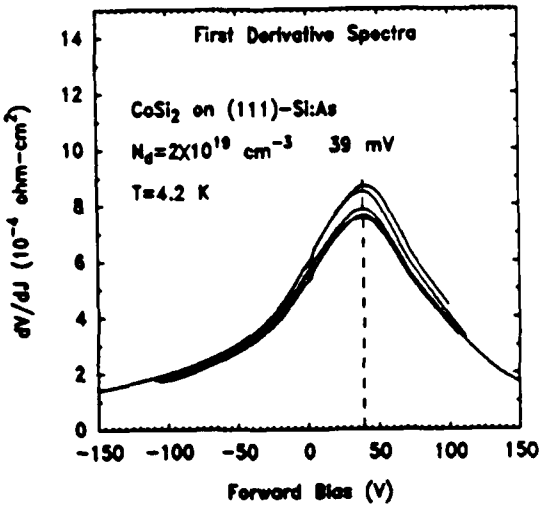

Fig. 3. Small-signal specific resistance vs. bias for various device sizes. The peak corresponds to the Fermi degeneracy *outside the Si depletion region.*

SUMMARY AND CONCLUSION

We have examined the electron tunneling spectra obtained from single-crystal epitaxial of $CoSi_2$, and type-A and type-B $NiSi_2$ films on degenerate n-type Si. Our results show direct evidence of k-conserving phonons assisting the transport of electrons from the semiconductor into the silicide. Strong peaks at TA and TO phonon energies corresponding to the wave vector of an indirect valley in Si are observed in forward bias for both $NiSi_2$ and $CoSi_2$. Somewhat weaker LO phonon peaks are also observed in both cases. The LA phonon peak is not observed in spectra obtained from $NiSi_2$ samples, but is sometimes weakly observed for $CoSi_2$ samples, along with other weak structure of unclear origin. In the reverse bias direction, the TA phonon is seen in $NiSi_2$ samples only, and is much weaker than and of opposite sign to the corresponding feature observed in forward bias. The inelastic tunneling component is very small compared to unassisted transport. Finally, measurements of dV/dI vs. V reveal an enhancement of n-type dopant concentration near the interface.

ACKNOWLEDGEMENTS

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Electrical behavior of GaAs–AlAs heterostructures

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We report an experimental study of the electrical behavior of GaAs–AlAs–GaAs heterostructures grown by metal–organic chemical vapor deposition. The structures consisted of a layer of AlAs several thousand angstroms thick sandwiched between layers of GaAs which were a few microns thick. The top layer of GaAs was doped degenerately *n*-type with Se, while the bottom layer was nondegenerately doped. Capacitance–voltage (C–V) and curent–voltage (I–V) curves were obtained as a function of temperature, illumination, and rate of data acquisition. Deep-level transient spectroscopy (DLTS) measurements were also made. The C–V showed hysteresis near zero bias with the capacitance being larger when the voltage was swept from reverse to forward bias in the dark. The C–V displayed a light sensitive peak near zero bias. With illumination, the capacitance was greater, and no hysteresis was observed. We explain these phenomena as being due to deep levels near the AlAs–GaAs interface; DLTS has confirmed this. I–V curves taken in darkness also showed hysteresis. We take this as further evidence of deep levels. Additionally, capacitance failed to level off in reverse bias, indicating a lack of inversion in the samples.

I. INTRODUCTION

Single barrier heterostructures are important constituents of many modern semiconductor devices. Structures as diverse as heterostructure transistors, quantum well lasers, and tunnel structures rely on the creation of barriers to electron transport.[1,2,3] These barriers are often realized by the epitaxial deposition of a wide band gap material in the midst of smaller band gap material, that is, with a heterostructure. The electronic properties of such constructions are thus of great importance.

We have studied GaAs–AlAs–GaAs heterostructures grown by metal–organic chemical vapor deposition (MOCVD). A variety of electrical measurement techniques were employed. These included capacitance–voltage (C–V), current–voltage (I–V), and deep level transient spectroscopy (DLTS) measurements. Our results may be summarized as follows. The C–V did not become constant in reverse bias, indicating a lack of inversion in the structure. The C–V also exhibited hysteresis near zero bias. The capacitance was larger when bias was swept from reverse to forward bias in the dark. With illumination the capacitance was larger, and no hysteresis was evident. These phenomena can be explained by the presence of deep electron traps near the AlAs–GaAs interface. DLTS measurements support this conclusion with direct evidence of these levels. I–V measurements show further evidence of deep levels, in that hysteresis was observed in these curves as well.

The samples we have studied can be generally classified as low current devices. This is because the barriers studied were fairly thick, and doping levels on the substrate side of the barrier were low. This was an advantage for the investigations reported here. In the case of C–V measurements, we were able to take C–V data over a large voltage range. In the case of I–V measurements, we were able to observe small effects, which might otherwise not be discernible. Finally, these samples were able to be examined with DLTS techniques. More conductive samples would have made this difficult.

II. EXPERIMENTAL

The results reported here are due to the study of several samples of the same basic geometry. Structures were prepared by an MOCVD technique.[4,5] The samples consisted of a single AlAs barrier sandwiched between layers of GaAs. The top layer of GaAs (nearest the surface) was between 1 and 3 μ in thickness and was doped degenerately with Se at $1\text{–}3\times10^{18}$ cm^{-3}. The GaAs layer on the substrate side of the barrier and the AlAs barrier itself were lightly doped with Se in one case and not intentionally doped in all other cases. In these cases, the dopant was likely Se as well, as this was the dopant for the substrate. C–V profiles of this region indicated an *n*-type doping of between 7×10^{15} and 3×10^{16} cm^{-3}. This region was several microns thick. Doping levels in the AlAs are not known. This region ranged between 1000 and 4000 Å in thickness. The substrate was made up of GaAs doped degenerately with Si at roughly 3×10^{18} cm^{-3}. A buffer layer of varying composition and thickness was grown on top of the substrate.

Photolithographic techniques were used to define Au–Ge contacts with diameters ranging from 70 to 450 μ. Contacts were isolated from each other by wet etching using a 4:1:1 solution of H_2SO_4, H_2O_2, and H_2O. Ohmic contacts were made to the top and bottom of the samples by evaporation of an Au–Ge alloy and annealing for 20–30 s at about 400 °C. Prepared samples were then attached to TO-5 transistor headers, using conductive silver paint. Electrical connec-

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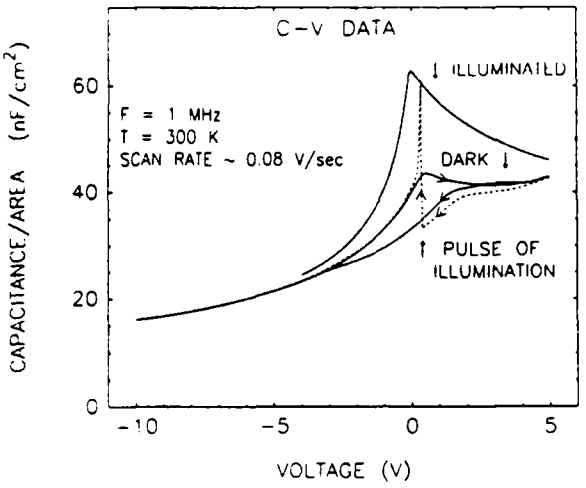

FIG. 1. Representative C–V data. The direction of sweep is indicated by arrows. Note the hysteresis in curves taken without illumination. The curve of large capacitance was taken under illumination and is comprised of two curves, one for both bias sweep directions. The dotted curve was taken with a pulse of illumination at the point indicated by the arrow. All data are taken at room temperature.

tions to measurement circuitry were made, using gold wire probes or wire bonds.

C–V and I–V measurements were made, using Hewlett Packard equipment. An HP4192 LF impedance analyzer was used for C–V measurements. An HP 4145 semiconductor parameter analyzer was used for I–V measurements. An HP 9816 computer was used to control both instruments. The impedance analyzer was capable of monitoring the phase angle of the measured impedance. This phase angle was monitored during the data acquisition process. C–V data presented in the figures were acquired digitally with a resolution of about 0.05 V and an effective sweep rate of about 0.083 V/s. I–V data were acquired point by point as well with the parameter analyzer averaging a large number of measurements before recording a data point. Acquisition rates for the presented I–V data were either 0.6 or 1.5 V/s. Rates were determined by independently measuring the time required to take a scan. Low temperature measurements were made, using an MMR Technologies refrigeration station. When data were taken under illumination, the illumination source was an incandescent lamp.

DLTS measurements were performed, using a method described by Lang.[6] An HP85 computer was used to control an MMR technologies refrigeration station. The computer was also used to acquire data from a double boxcar integrator, which sampled the capacitance output from a Boonton 72DB capacitance meter operating at 1 MHz. The method is similar to that employed by previous workers in this laboratory.[7]

We now describe general features of the data to be discussed. Reverse bias denotes negative voltage on the top layer of degenerately doped GaAs. Forward bias refers to positive voltage on the top layer. Capacitances are quoted in units of nanofarads per square centimeter. Currents are in picoamps. Finally, the AlAs–GaAs interface refers to the interface between the AlAs and the low doped GaAs layer

III. RESULTS

A. Capacitance results

In Fig. 1, we present data representative of the C–V behavior of all the samples represented in this article. Some of these results have been presented previously.[8] Initially, one observes that the capacitance does not level out in reverse bias. This implies that the depletion region is continuing to expand. This continues to occur to the breakdown voltage of the device, which was usually about 25 V, but was as large as 50 V in one case. One can conclude from this that no inversion takes place in this structure. This is explained as being due to poor confinement of minority carriers by the AlAs valence band.[9]

Near zero bias, hysteresis is evident in C–V curves taken without illumination. When voltage is swept from forward to reverse bias, the capacitance is observed to be lower than when bias is swept the other way. This indicates a nonequilibrium process. This behavior can be explained by the presence of electron trap levels spatially localized near the AlAs–GaAs interface. Empty traps, being positively charged, contribute to the voltage in the depletion region, whereas filled traps do not. The capacitance at zero bias will be different, depending upon the initial charge state of the deep levels. The absence of such hysteresis has been used as evidence for the lack of deep levels in similar structures.[10]

Consider first the case in which bias is swept from reverse to forward bias in the dark. In this case, electron traps in the depletion region will be empty. There will not be a significant number of electrons near the trap levels until the depletion edge, which is a few extrinsic Debye lengths wide,[11] nears the trap levels. They then begin to fill, thus necessitating additional depletion of free carriers and a consequent decrease in capacitance. This decrease stops when the trap levels return to equilibrium with applied bias.

The levels are initially filled when voltage is swept from forward to reverse bias. When the depletion region sweeps over the trap levels, they begin to empty. This process is, in the absence of illumination, a thermal one. When voltage is swept fast enough, the population of filled levels is not in equilibrium with the applied bias. Some levels that were empty when voltage was swept the other way are now filled, thus requiring additional free carrier depletion and a lower capacitance. The two curves meet when the number of empty levels increases to an equilibrium level. When data are taken very slowly, both the hysteresis and the peak in the capacitance are no longer evident.[8]

In Fig. 1, we also present data taken under illumination. In this case, there is no hysteresis. This is because light provides a nonthermal means to empty the trap levels. Overall capacitance is greater, because charge in the depletion layer is increased by the light. A peak in the capacitance continues to be observed. This is because the number of electrons near the traps continues to change as the depletion width sweeps across the spatial position of the levels.

One further C–V curve is presented in Fig. 1. Voltage was swept from forward to reverse bias in this curve. At the start of the curve, trap levels are filled and the C–V curve is parallel to the reverse going curve. At about 0.3 V, the sample was

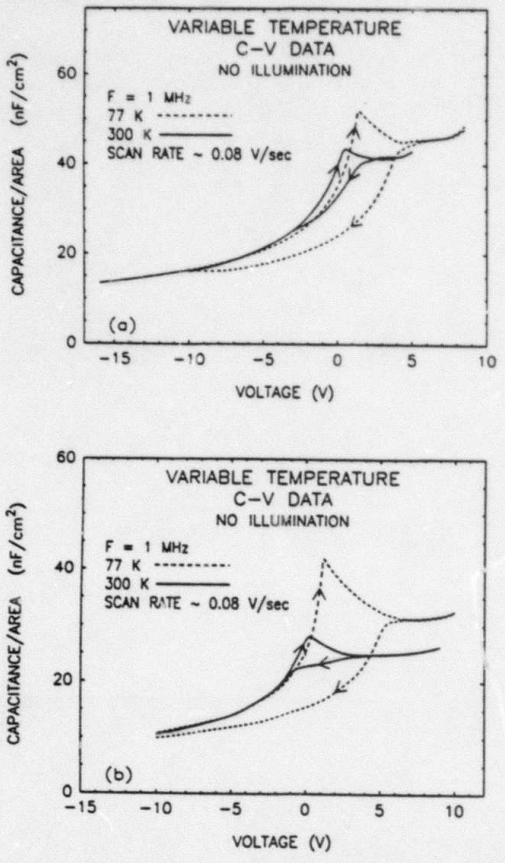

FIG. 2. C–V curves for two samples at 300 and 77 K. Note the increase in hysteresis for 77 K curve and the shift of the peak to more forward bias. The direction of sweep is indicated by arrows.

briefly exposed to illumination. Trap levels are emptied, and photoexcited carriers are created. The capacitance, therefore, rises to its illuminated value. The illumination ceases, and the capacitance decays, due to the relaxation of photoexcited carriers. In the illustrated case, the depletion edge has already crossed the position of the trap levels. This means that the traps remain empty. Therefore, the capacitance relaxes to values associated with the *forward* going curve. This experiment serves to verify the explanation presented for the C–V behavior of the samples. It links all three curves together, reverse going, illuminated, and forward going.

For one sample, the hysteresis effect was investigated as a function of frequency at room temperature in the dark. The hysteresis effect was seen to remain almost constant for ac oscillator frequencies ranging from 10 kHz to 5 MHz. In fact, the entire C–V curve was changed very little by varying the measurement frequency. This can be taken to mean that the emission rate of the traps is far below this frequency range.

In Fig. 2, we present C–V data for two samples at 300 and 77 K. The hysteresis described previously increases as temperature decreases. Additionally, the peak in the forward going curve shifts to more positive voltage and is more pronounced. This can be explained by the longer emission time of the deep levels and the more sharply defined depletion edge, both of which are obtained at lower temperatures.

One can gain some insight into the nature of the deep levels from the data presented in Fig. 2. Initially, one observes that they must be electron traps, since they are positively charged when empty. Also, one observes that their emission time should be quite long. Rough estimates would indicate several seconds at room temperature. A rough concentration estimate can be made from the difference in capacitance between forward and reverse going curves. The total capacitance is the series combination of the AlAs and the GaAs depletion layer capacitances. At the bias at which the forward going curve is peaked, we have

$$\frac{1}{C_1}=\frac{1}{C_i}+\frac{w_1}{\epsilon_s},$$

where C_1 is the capacitance of the forward going curve at this point, C_i is the saturation capacitance of the AlAs in forward bias, w_1 is the depletion width, and ϵ_s is the dielectric constant of GaAs. Similarly, for the reverse going curve, at the same bias,

$$\frac{1}{C_2}=\frac{1}{C_i}+\frac{w_2}{\epsilon_s}.$$

Solving for the difference in depletion width $\delta w = w_2 - w_1$:

$$\delta w=\frac{(\delta C)\epsilon_s}{C_1 C_2},$$

where $\delta C = C_1 - C_2$. We equate the carrier density, $N_d(\delta w)$, contained in this region to the deep level sheet concentration:

$$N_d(\delta w)=N_t.$$

This estimate yields concentrations in the 10^{11} cm^{-2} range for both samples in Fig. 2 at 77 K. Concentration estimates are somewhat lower (less than an order of magnitude) when made at 300 K. This is due to the longer trap emission time obtained at low temperature.

In Fig. 2, the saturation capacitance is observed to change as temperature changes. In forward bias, conventional theory[12] dictates that the capacitance should level off at approximately

$$C=C_i=\frac{\epsilon_i}{d},$$

where ϵ_i is the dielectric constant of AlAs, and d is the thickness of the AlAs. Barrier thickness for the sample in Fig. 2(b) was measured with a scanning electron microscope (SEM) to be about 2500 Å. The thickness prediction at 77 K is about 2800 Å. At 300 K, the thickness prediction is about 3600 Å. The decrease in predicted thickness between 300 and 77 K is suggestive of negative charge in the barrier. That is, the AlAs is slightly p type. Ionized acceptors could deplete parts of the GaAs, thus resulting in a lower saturation capacitance than that of the AlAs alone. As temperature goes down, the number of ionized acceptors decreases, thus decreasing the amount of depletion and raising the saturation capacitance. Donor density for the sample in Fig. 2(a) is larger than that for Fig. 2(b). This is consistent with the observation that Fig. 2(a) does not show as much change in saturation capacitance as Fig. 2(b). It further suggests that

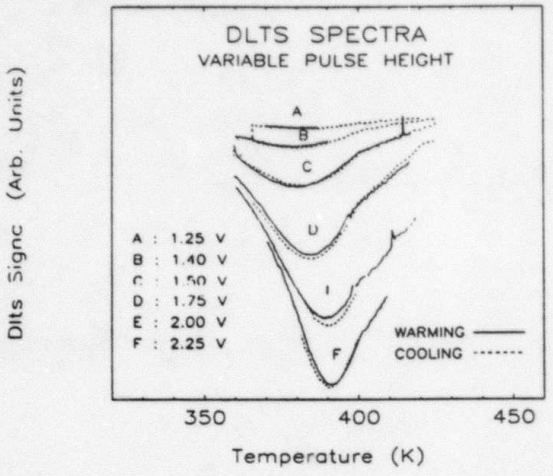

FIG. 3. DLTS curves for a variety of labeled pulse heights. Quiescent reverse bias, pulse width, and rate windows are held constant. Warming and cooling spectra are both presented. Quiescent reverse bias is − 1.0 V. Note the peak shift.

acceptor density may be larger for the sample of Fig. 2(b).

When a sample with a barrier doped heavily with Mg was studied, the discrepancy between predicted and SEM measured barrier thickness was quite large. Room temperature C–V predicted about 4000 Å, whereas the SEM showed the barrier thickness to be about 1000 Å. A rough calculation, treating the junction between the AlAs, doped at 1×10^{18} cm^{-3}, and the GaAs, doped at 1×10^{16} cm^{-3}, as a simple p^+n junction, yields sufficient depletion to achieve the observed result.[12]

Finally, one sample was studied in which the barrier was intentionally doped n type, while all other sample parameters remained unchanged. This sample showed much higher levels of conduction than those reported here. One can generalize these results to conclude that all the samples reported on here had barriers which were more or less p type. This sort of general information about the barrier itself is valuable, because barrier composition information is difficult to obtain. More generally, these results suggest that band bending is a very important factor in determining the conductivity behavior of barrier structures.

B. DLTS results

DLTS studies were performed on two samples. The basic results of the DLTS measurements corroborate and expand the observations of the C–V studies. Only general information will be taken from the data presented. Electron trap levels were observed. These levels were observed to be localized near the interface with possible extension into the AlAs. Evidence for interface state presence or multiple spatially localized deep levels was observed. Activation energy plots were made for both samples, which suggest that the same level was seen in both cases.

In Fig. 3, we present a series of DLTS spectra of one sample. The variable parameter in these scans was the magnitude of the pulse. The pulse duration, quiescent reverse bias, and rate windows were not changed. One observes that the size of the DLTS peak increases as the pulse height increases. Further, the peak of the spectra increases with the pulse height. No trap signature was observed for pulse heights below 1.0 V at a quiescent reverse bias of 1.0 V. Indeed, the trap signature at this level was extremely small. This bias corresponds to a depth of about 1500 Å from the barrier. This means that the trap levels extend less than this distance into the GaAs. As the quiescent bias level was brought into forward bias, the trap signature decreased. This indicates that the deep levels are isolated near the AlAs–GaAs interface. However, the extent to which the AlAs was scanned is not known. Therefore, it is not possible to say how far into the AlAs these levels extend.

The significance of the observed peak shift is as follows. For a conventional metal–insulator semiconductor (MIS) structure, increasing pulse height allows additional regions of the interface to be scanned. If interface states are present in the energy gap, additional states will be able to participate in the DLTS emission process as the pulse height increases. This will change the shape of the DLTS capacitance transient and the peak of the DLTS spectrum shifts. Therefore, observation of peak shift in a series of DLTS spectra of an MIS structure is indicative of interface states.[13] The structures we have studied are not pure MIS structures. Therefore, one cannot say conclusively that the observed peak shift indicates their presence. The shift could be due to other things as well. More than one bulk level could produce the effect. Both bulk levels and interface states may be present; this is often the case.[14,15] Factors, such as interdiffusion at the AlAs–GaAs interface, could also be important.

Using a standard method,[6,14,15] trap concentration can be obtained. This method, which relates trap concentration to the variation of the DLTS peak with pulse height, is not accurate for deep level concentrations approaching that of the shallow level. C–V analysis has shown that the trap level concentration could be this large. Thus, the rough estimate of trap concentration of 1×10^{15} cm^{-3} one gets from this method is probably below the actual concentration.

In Fig. 4, activation energy plots for the deep levels observed, corrected for the T^2 exponential prefactor, are presented. These plots are informative, even though the peak in the DLTS spectra represented by each point of the plot is subject to the peak shift phenomena described above. First, the possible peak shift is not very large. Second, the data from the two samples are very similar. This suggests that the same level is being observed in *all* samples.

Figure 4(a) yields an activation energy of 500 meV with a standard error of 70 meV and a capture cross section of 6×10^{-18} cm^{-2}. Figure 4(b) also yields an activation energy of 500 meV with a standard error of 40 meV and a capture cross section of 1×10^{-17} cm^{-2}. Owing to the limited range of emission rates obtained, the capture cross section data are not very accurate. These data yield emission times of several seconds. This is in good agreement with capacitance data.

C. Current–voltage results

I–V measurements were made on all samples. Measurements were made with and without illumination. When not illuminated, the currents typically observed were below a

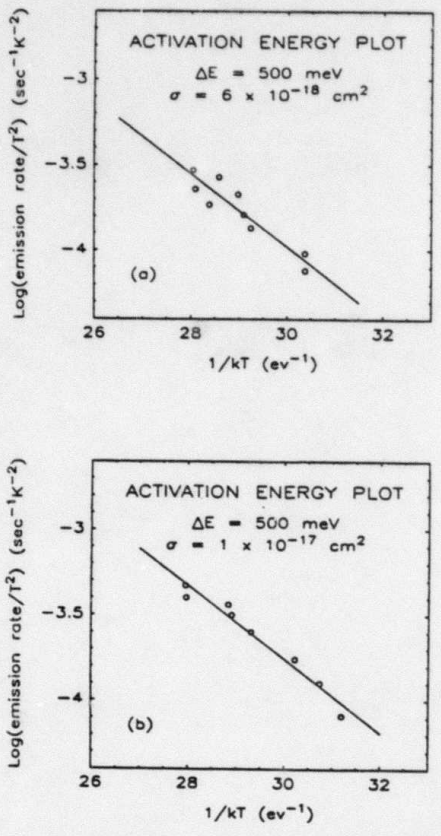

FIG. 4. T^2 corrected activation energy plots for two samples. ΔE is the activation energy. Standard error in ΔE is 70 meV for (a), and 40 meV for (b). σ is the capture cross section. Both samples show the same activation energy. This implies that the same trap is present in both samples.

nanoamp. Hysteresis was observed in the I–V curves of all samples studied. This hysteresis was investigated as a function of rate, temperature, and illumination. When illuminated, currents are much larger, and no hysteresis is observed.

In Fig. 5, we present a representative I–V curve. No light falls on the sample in the pictured voltage range. Consider the curve obtained by sweeping voltage from negative to positive values. With the sample in reverse bias, it was briefly exposed to light. As voltage becomes positive, a sudden increase in current is observed. This increased current is maintained at an almost constant level until large scale conduction begins. This is not observed when the I–V curve is taken with bias swept from forward to reverse values.

This result can be explained by the same deep levels whose presence was evidenced by C–V and DLTS studies. If the sample is illuminated in reverse bias, trap levels are emptied. This pulse of light serves to provide a known initial state for the trap levels, making analysis simpler. As voltage is swept toward forward bias, some levels will fill, but most will remain empty. As the depletion edge crosses the spatial position of these empty levels, they begin to fill. As they fill, the number of electrons in the measuring circuit decreases. This time rate of change of carriers is the current enhancement observed.

When the data are taken starting from forward bias, the aforementioned deep levels are filled at the outset. As the depletion region envelopes the deep levels, they begin to thermally empty. This process does not produce a sudden increase in the number of carriers. Therefore, no jump in current is observed when data are taken this way.

An estimate of the number of deep levels required to create this effect can be made. The area under the enhanced current part of the I–V curve can be approximated as a rectangle. The area of this rectangle can be converted to a charge, and, hence, to a sheet concentration as

$$N_t = \frac{I_s(\delta V)}{ARq},$$

where I_s is the height of the current step, δV the voltage range over which the enhanced current persists, A is the area of the device, R is the rate at which voltage is changed, and q is the electronic charge. The devices pictured in Figs. 5 and 6 were 350 μ in diameter. Taking 40 pA as the size of the current step in Fig. 5, and 2 V as the voltage range, we obtain a concentration of about 3×10^{11} cm^{-2}. This agrees well with the estimates of concentration made from C–V data.

In Fig. 6, we present variable temperature I–V curves for one sample. Two different rates are presented. The faster rate, in Fig 6(b), is obtained with less averaging by the parameter analyzer and is thus noisier. These data show how the hysteresis effect varies with temperature. The data were obtained by illuminating the sample briefly, during reverse bias. The spatial location and energetic position in the gap of the levels will both play a role in determining the voltage at which the enhanced current begins. This onset voltage is very sensitive to the point at which illumination was applied in reverse bias. The reason for this is that the time at which the sample was last illuminated will influence both the number and the location of empty levels available to participate in the effect. The variation in the onset voltage shown in Fig. 2 is due to this effect. No systematic variation with temperature of this onset voltage was observed.

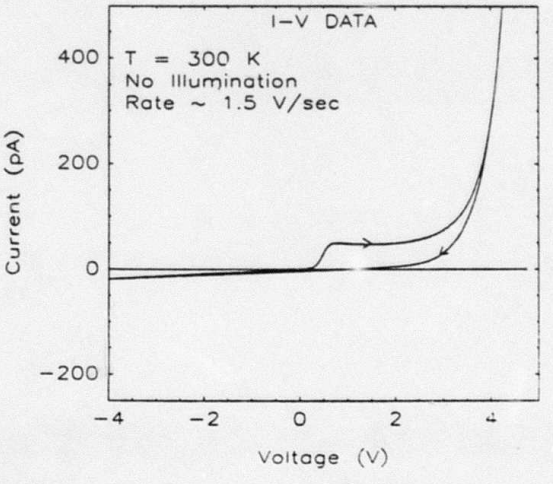

FIG. 5. I–V curves for one sample at room temperature. Direction of sweep is indicated by arrows. In the forward going sweep, trap levels were emptied at about -5 V by brief exposure to illumination. The hysteresis is due to trap filling effects.

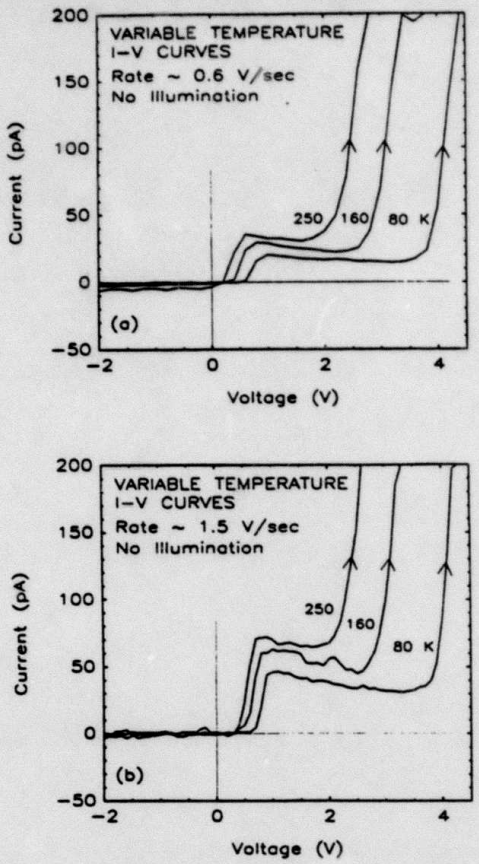

FIG. 6. Variable temperature I–V curves for the same sample at different rates. Note the increase in size of current jump as rate increases. Note also the decrease in current jump with temperature, at a given rate. To empty levels, devices were exposed to brief illumination at a bias of about -4 V. Greater noise is observed in (b) because of decreased data averaging.

It is seen in Fig. 6 that the height of the current step decreases as temperature decreases. This can be explained by the general decrease in current as temperature goes down. There are fewer electrons passing over the trap levels, and, thus, the number which drop into traps to supply additional current is smaller as well. Also, one observes that the onset of large scale conduction of the device advances to more positive voltages as temperature goes down. Thus, the voltage range over which hysteresis is observed is seen to increase. These two effects combine to keep the trap concentration estimate (as calculated above) roughly constant in the 10^{11} cm^{-2} range.

As the acquisition rate increases, the current jump becomes larger. This can be seen by comparing Fig. 6(a) to Fig. 6(b). This is because a faster sweep rate allows a more rapid change in the carrier population. This increased rate of change in the number of carriers results in a larger current jump. Conversely, the current jump goes to zero as the rate decreases to very slow values. Since the same number of traps are being filled in each case, the trap concentration estimate, obtained as above, is about the same for Figs. 6(a) and 6(b).

IV. CONCLUSIONS

We have studied the behavior of MOCVD grown GaAs–AlAs–GaAs heterostructures, using C–V, DLTS, and I–V measurements. These three methods combine to provide some information about the samples studied. They are low current structures, having a slightly p-type barrier; they do not exhibit inversion. The samples exhibit light sensitivity in both the C–V and the I–V. There are deep electron trap levels associated with the AlAs–GaAs interface with less than 1500 Å extension into the GaAs and possible extension into the AlAs. The sheet concentration of these levels is in the low 10^{11} cm^{-2} range.

Results of this study can have significant impact on MOCVD grown devices, using structures of this type. The observed lack of inversion poses problems for p-channel field effect transistors. High electron mobility transistors (HEMT's) and any other device relying upon conduction alongside the barrier of a structure of this type will suffer efficiency losses due to the observed trap levels. The observed hysteresis is an interesting memory effect, which could be an important consideration in the behavior of low current devices.

ACKNOWLEDGMENTS

We would like to acknowledge A. R. Bonnefoi, D. H. Chow, R. J. Hauenstein, R. S. Bauer, T. L. Paoli, and F. A. Ponce for valuable discussions. We would also like to acknowledge the technical assistance of H. Chung, F. Endicott, D. Taylor, T. T. Tjoe, M. Bernstein, W. Mosby, T. Anderson, and J. Tramontana. One of us (T.K.W.) is grateful to acknowledge I.B.M. for financial support. Parts of this work were supported by DARPA under Contract No. N00014-84C-0083.

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PAPER 9

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PHOTORESPONSE OF ASYMMETRICALLY DOPED GaAs-AlAs HETEROSTRUCTURES UNDER EXTERNAL BIAS

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ABSTRACT

We present new experimental results in the photoresponse behavior of GaAs-AlAs-GaAs heterostructures. Structures consisted of a layer of AlAs several thousand angstroms thick sandwiched between layers of GaAs which were several microns thick. The layer of GaAs nearest the surface was doped degenerately *n* type, whereas, the layer beneath the AlAs was doped non-degenerately *n* type. The asymmetric doping and the AlAs layer are shown to play an important role in determining the photoresponse. We present photocurrent per incident photon data, as a function of incident light energy, at a variety of external biases. We also present current voltage curves taken while samples were illuminated by an incandescent lamp. Zero bias photocurrent consistent with electron transport from the non-degenerate region beneath the AlAs to the degenerate region forming the surface is observed. As negative voltage is applied to the top of the sample, this photocurrent changes sign. These results are explained by introducing the concept of a "collecting interface" to account for fields and scattering in the AlAs. Further, we explain why the shape of the photocurrent spectrum depends upon the sign of the photocurrent.

Photoresponse techniques are powerful tools for investigating the properties of heterostructure materials. In this letter we present new information about the photoresponse of GaAs-AlAs-GaAs heterostructures. Previous papers have reported the photoresponse of symmetrically doped GaAs-AlAs-GaAs heterostructures grown by metalorganic chemical vapor deposition (MOCVD).[1-4] These structures were characterized by thin (50-250 Å) AlAs barriers and degenerate *n* type GaAs layers. In this letter, we use similar techniques to investigate asymmetrically doped GaAs-AlAs-GaAs heterostructures grown by MOCVD, having thick (1000-3000 Å) AlAs barriers. The structural differences are important because they allow the AlAs layer to play a much more important role in determining the photoresponse of the overall structure. This permits a more complete picture of the photoresponse of GaAs-AlAs-GaAs heterostructures

Basic results are summarized as follows. Zero bias photocurrent measurements reveal that illumination of the front of the sample produces photocurrent whose sign is consistent with electron transport from the back to the front of the sample. This new observation differs from previous results, wherein front to back electron transport was observed[1-4] and prompted us to examine the photocurrent as a function of applied bias. When negative voltage is applied to the top of the sample, photocurrent changes sign and grows in magnitude, becoming consistent with front to back electron transport. Positive bias does not cause a sign change in photocurrent from the zero bias case. The size of the barrier and the asymmetric doping on either side of it make the concept of a "collecting interface" important in explaining these observations. Current voltage *(I-V)* data are helpful in visualizing the overall behavior and are included. Additionally, the shape of the photocurrent spectrum, including the location of the peak, depends upon the sign of the photocurrent. We explain this new result in terms of structural properties of the samples studied. Studies were performed at room temperature, except where specifically noted.

Several samples were studied, all of which showed similar behavior. We focus on the

specific behavior of two samples. Structures were grown by an MOCVD technique.[5,6] The samples studied consisted of a single AlAs barrier sandwiched between layers of GaAs. The substrate was made up of GaAs doped degenerately with Si at about 3×10^{18} cm^{-3}. A buffer layer of varying composition and thickness was grown on top of the substrate. For sample 1, the GaAs top layer was 3.6 microns thick and was doped degenerately n-type with Se at about 3×10^{18} cm^{-3}. The GaAs layer underneath the AlAs was doped n-type at 3×10^{16} cm^{-3} with Se and was about 3 microns thick. The doping in this layer was estimated during growth from the growth parameters and confirmed with capacitance voltage (C-V) profiles. The AlAs layer was estimated from growth parameters to be about 2500 Å thick and doped lightly with Se. Doping levels in the AlAs are unknown. For sample 2, the GaAs top layer was 4.35 microns thick and was doped degenerately n-type with Se at about 1×10^{18} cm^{-3}. The AlAs layer and the GaAs layer beneath it were not intentionally doped. C-V profiles of the GaAs layer showed it to be doped n-type between $7 - 9 \times 10^{15}$ cm^{-3}. This GaAs layer was about 3 microns thick. Doping in the AlAs is unknown. The AlAs layer was about 2500 Å thick.

Photolithographic techniques were used to define mesas with diameters of 350 microns. Ring shaped Au-Ge ohmic contacts were placed on these mesas, allowing light to enter the device without passing through the contact material. Detailed sample preparation information exists elsewhere.[1-4] I-V measurements were made, using an HP 4145 semiconductor parameter analyzer under computer control.[7] Forward bias refers to positive voltage on the top layer of degenerately doped GaAs. Positive current refers to positive charge flow from front to back of the sample. Positive current is observed in forward bias. Photocurrent data were obtained by directing light from a 1000 W quartz halogen lamp through a SPEX 1269 spectrometer, the output of which was chopped at 27 Hz, and focusing through a microscope objective onto the sample. Synchronous detection of the current arising from this illumination, using a current sensitive preamp and a lock-in amplifier, assured that

only the photocurrent was measured. External biases were applied with an HP 6002A DC power supply. Direct measurement of the sign of the photocurrent (or photovoltage) was made, using an oscilloscope or a voltmeter. At each wavelength, the photocurrent thus obtained was divided by a measure of the incident photon density to obtain photocurrent per incident photon.

In Fig. 1, we present an I–V curve for sample 2 at room temperature. This curve, taken under illumination from an incandescent source, is representative of the I–V behavior of all samples studied. Current enhancement due to the light is observed. Currents are about three orders of magnitude larger than when not illuminated.[7] In forward bias, positive current enhancement is observed. In reverse bias, negative current enhancement is observed. It is interesting to note that the zero bias photocurrent is positive, consistent with electron flow from the back of the sample to the front. I-V curves of this type, taken at temperatures ranging from 80 °K to 325 °K, continue to show positive current at zero bias. This differs from earlier results.[1–4]

Free carrier absorption in the conduction bands of the GaAs is responsible for producing the observed photocurrents. Such absorption, which involves a phonon, can result in carriers being directed toward the barrier with energies greater than the conduction band offset of the AlAs. Carriers which travel from one side of the AlAs to the other contribute to photocurrent.

In thin barrier samples that are symmetrically doped, the driving force behind the photovoltage is explained very well as being due to differences in the number of optically excited carriers between the two GaAs layers. This succeeds in explaining the photoresponse of such structures for two reasons. First, little energy loss can take place across the thin barrier. Also, the symmetric doping ensures that at zero bias the AlAs conduction band edge will be at the same energy at both interfaces.

In the samples studied here, the AlAs plays an important role. The AlAs is thick enough to allow significant energy loss to take place across it. This makes the presence of an electric field in the AlAs important. Depending on the bias conditions, the conduction band edge of the AlAs will be at a higher energy at either interface (a), or interface (b), as labeled in the inset of Fig. 1. If the interface happens to be the AlAs-GaAs interface (interface (b) in the figure), then electrons from the back will be collected as soon as they cross this barrier, whereas, electrons from the front must cross the entire AlAs region before reaching the highest energy barrier. Also, positive external bias will increase the height of this barrier, as seen by front side electrons. We have two interfaces, but only one is important for current collection. It is the concentration gradient across this "collecting interface" that drives the photocurrent. We observe that at zero bias, there is a built-in voltage across the AlAs, due to the doping asymmetry in the structure. This identifies interface (b) as the collecting interface and explains why positive photocurrent is observed at zero applied bias. The photoenhanced current is larger in reverse bias, because band bending causes the collecting interface to shift to position (a) in the inset of Fig. 1, where the number of electrons and photons are greater than at (b). Scattering, accumulation, and depletion effects in the GaAs layers can also be important in affecting the population of excited carriers at the collecting interface. For example, forward bias results in some accumulation of electrons near interface (b), thus increasing the number of electrons available for photoexcitation.

In Fig. 2 and Fig. 3, we present plots of the magnitude of the photocurrent, as a function of incident light energy at a variety of external bias levels. The sign of the photocurrent is negative for reverse bias scans and positive for zero and forward bias scans. At about 150 mV of reverse bias, the photocurrent spectra are double peaked and two-signed. The photocurrent is negative in sign near the lowest energy peaks and positive near the higher energy peaks. Relative intensities are accurately represented.

Structural information is contained in the spectra of Fig. 2 and Fig. 3. We now discuss features common to data presented in both figures. As in earlier studies[1-4], holes are not responsible for the observed currents. The main evidence for this is that sizable signal appears at energies at which holes are not created in the structure. Optical properties of the samples determine the peak position in the spectra of Figs. 2 and 3. A peak is observed when the difference in optically excited carriers is most favorable to the production of photocurrent of the observed sign. As in earlier studies, little signal is observed at long and short wavelengths. This is because the difference in optically excited carriers across the important interface is not as large as at other wavelengths.

For reverse bias scans, we can predict the location of the peak. The doping asymmetry in the samples means that there will be a range of energies over which band-to-band absorption can take place in the low doped layer of GaAs but not in the degenerately doped top layer. By reducing light intensity, band-to-band absorption will decrease the number of optically excited free carriers. Therefore, the difference in photoexcited carriers will be most favorable to front to back electron transport when incident light energy is equal to the band gap of the low doped material. This is observed, in that all samples studied exhibited reverse bias photocurrent peaks at about 1424 meV.

Zero and forward bias photocurrent spectra are observed to be peaked at higher energies than reverse bias spectra. This can be qualitatively explained. We have seen that front-to-back electron transport is most likely when the incident light is at the bandgap energy of the low doped material. As energy increases from this value, band-to-band absorption begins to decrease the number of optically excited free carriers in the top layer. This changes the concentration difference across the collecting interface to one more favorable to back-to-front electron transport (positive photocurrent). At energies greater than the sum of the bandgap plus Fermi degeneracy of the top layer, strong absorption occurs near the surface of the sample, decreasing light intensity near the barrier. Between

these two energies, there will be a point of maximum favorability to electron transport from back to front. Thus, we conclude that the photocurrent peak should lie at higher energies in forward bias than reverse bias, but less than the bandgap plus degeneracy of the top layer.

Since the photocurrent is sometimes positive and sometimes negative, there must be a bias at which photocurrent is small. This bias level is about -150 mV for samples 1 and 2. At this bias, the sign of the photoresponse depends on the energy of the incident light. At light energies most favorable to negative photocurrent (near 1424 meV), one observes negative photocurrent. At other energies, the photocurrent is positive. In addition, the photocurrent at very short wavelengths is small and negative.

We now discuss the differences between Fig. 2 and Fig. 3. Most differences can be ascribed to the differences in doping between the two samples. This is because the barrier thicknesses are the same. Note that the general peak-to-background ratio is higher for sample 1 than for sample 2. This can be explained by the higher doping levels in sample 1. This would tend to increase the peak photocurrent in both directions. Note also that the shift in peak position between forward and reverse bias spectra is significantly greater for sample 1 than for sample 2. The peak shift for sample 1 is about 28 mV, but, it is only 9 mV for sample 2. Higher doping results in a greater difference between band-to-band absorption onsets in the two layers. This leads to a larger peak shift.

A structure similar to sample 2, but with a 1000 Å AlAs barrier was studied. In this case, only about 30 mV of bias was needed to produce negative photocurrent. This is due to the decreased energy loss across the thinner AlAs layer. The effect is to reduce the amount of applied bias necessary to produce negative photocurrent. For much thinner structures, one would expect to see positive photocurrent at zero bias. This demonstrates consistency with earlier reports.[1-4]

It should be noted that these samples have significant electron trap level densities near the interface of the AlAs with the low doped GaAs layer.[7,8] These levels do not change the basic explanation for the observed results. They may, however, provide a means of increasing the free carrier population in the low doped GaAs layer. Increases in this population can effect the photoresponse, because they increase the free carrier absorption probability. Conclusive evidence of the role of deep levels in the photoresponse of these structures requires further study. Finally, it should also be noted that the loss properties of the barrier could depend to some degree on the intensity of light in the barrier region.

We have presented an experimental study of the photocurrent behavior of asymmetrically doped GaAs-AlAs-GaAs heterostructures characterized by thick AlAs barriers. New results are observed, which can be explained with basic structural properties of the samples. Doping asymmetries are reflected in the magnitudes of the observed photocurrents. These asymmetries, coupled with the thick AlAs barriers, are also evidenced in the observation of positive photocurrent at zero bias. The photocurrent is seen to change sign when the structures are reverse biased. The concept of a "collecting interface" is introduced to account for the effects of fields and scattering across the AlAs. Trends are established which demonstrate consistency with earlier work.

We are pleased to acknowledge the work of T.E. Schlesinger done, together with R.T. Collins and A. Zur, in this laboratory with the same basic setup used here. We are grateful to R.J. Hauenstein, A.R. Bonnefoi, D.H. Chow, R.S. Bauer, and T.L. Paoli, for valuable discussions. We would also like to acknowledge the technical assistance of H. Chung, F. Endicott, D. Taylor, T.T. Tjoe, M. Bernstein, W. Mosby, T. Anderson, and J. Tramontana. One of us (T.K.W.) is grateful to acknowledge International Business Machines Corporation for financial support. Parts of this work were supported by the Defense Advanced Research Projects Agency under contract No. N00014-84C-0083.

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FIGURE CAPTIONS

FIG. 1. (a) I-V data for sample 2 taken under illumination at room temperature. Zero bias photocurrent is consistent with electron transport from the back of the sample to the front. Forward bias in the figure denotes positive voltage on the top of the sample. The inset shows a schematic band diagram for the structure at zero bias. The schematic is not drawn to scale, does not include band bending, and is presented as a conceptual aid only. Labels (a) and (b) in the inset refer to the two interfaces.

FIG. 2. Plots of the magnitude of the photocurrent per incident photon for sample 1 at a variety of external biases. Relative intensities are correctly represented. The -0.148 V scan has positive and negative components. Zero and +2.00 V scans are positive in sign. -0.30 and -0.50 bias spectra are negative in sign.

FIG. 3. Plots of the magnitude of the photocurrent per incident photon for sample 2 at a variety of external biases. Relative intensities are correctly represented. The -0.147 V scan has positive and negative components. Zero and +2.00 V scans are positive in sign. The -0.30 V spectrum is negative in sign.

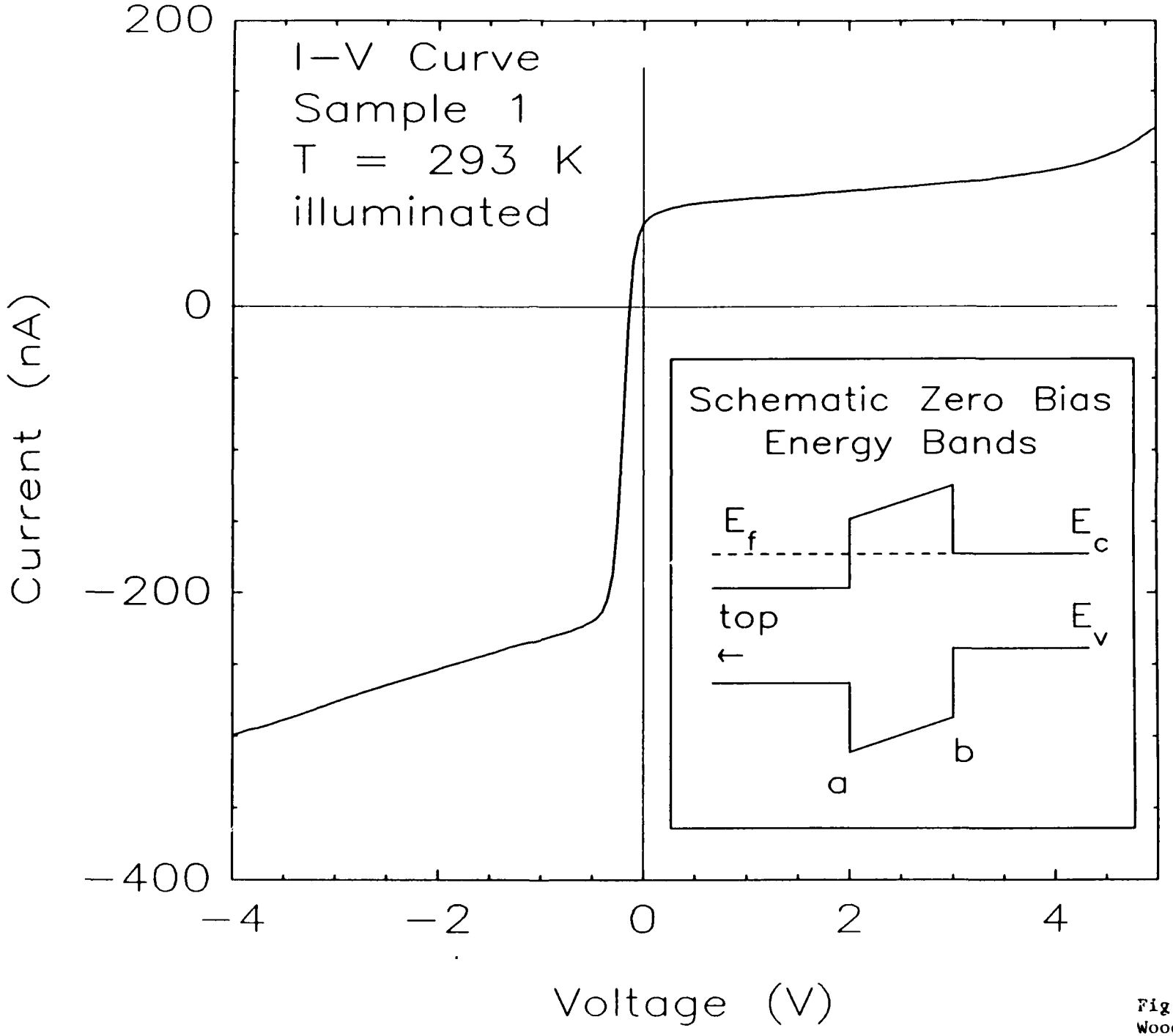

Fig. 1
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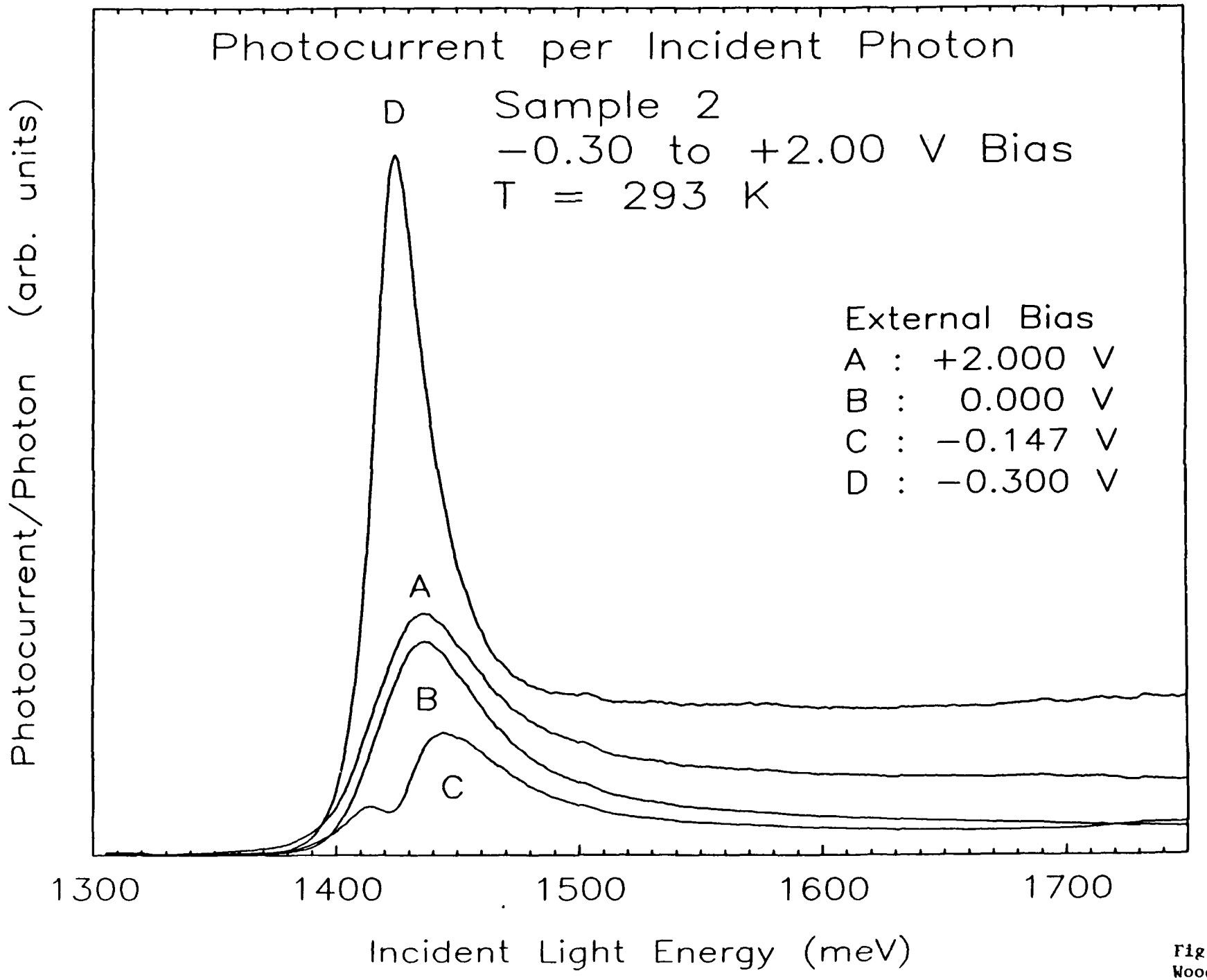

Fig. 2
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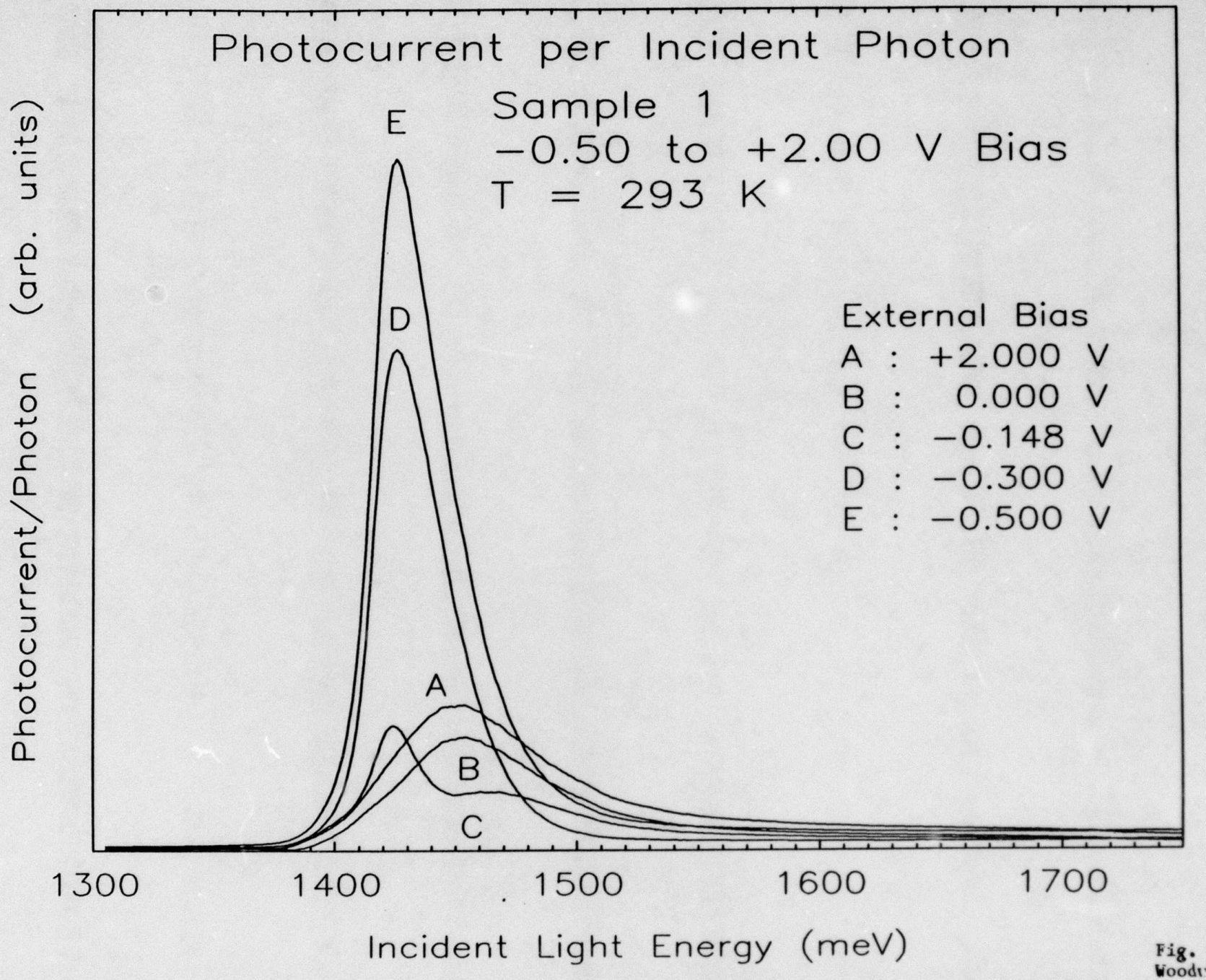

Fig. 3
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Capacitance-voltage characteristics of GaAs-AlAs heterostructures

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PAPER 10

We report on an experimental study of the temperature and photosensitive capacitance-voltage (C-V) characteristics of GaAs-AlAs-GaAs heterostructures grown by metalorganic chemical vapor deposition. The structures consisted of a layer of AlAs either 2500 or 4000 Å thick sandwiched between layers of GaAs which were a few microns thick. C-V curves were measured at 1 MHz, both with and without illumination. Measurements were made at 77 and 300 K. The C-V showed hysteresis near zero bias with the capacitance being larger when the voltage was swept from reverse to forward bias in the dark. The C-V displayed a light sensitive peak near zero bias. With illumination, the capacitance was greater, and no hysteresis was observed. We explain these phenomena as being due to deep levels near the AlAs-GaAs interface.

Many modern electronic devices are based on single-barrier semiconductor heterostructures. The electrical properties of such structures are thus of significant interest. The capacitance versus voltage (C-V) behavior can be used to determine basic electronic behavior of the structures,[1-3] such as doping profiles, barrier thicknesses, as well as band offset values.[4]

We have studied the basic capacitance behavior of two structures grown by metalorganic chemical vapor deposition (MOCVD). The basic results of this letter may be summarized as follows. The C-V curves did not level out in reverse bias, indicating a lack of inversion in the samples. The C-V showed hysteresis near zero bias with the capacitance being larger when the voltage was swept from reverse to forward bias in the dark. The C-V displayed a light sensitive peak near zero bias. With illumination, the capacitance was greater, and no hysteresis was observed.

Structures were prepared by an MOCVD technique.[5,6] The samples studied consisted of a single AlAs barrier sandwiched between layers of GaAs. The substrate was made up of GaAs doped degenerately with Si at roughly 3×10^{18} cm^{-3}. A buffer layer of varying composition and thickness was grown on top of the substrate.

For sample 1, the GaAs top layer was 3 μm thick and was doped degenerately n type with Se at about 3×10^{18} cm^{-3}. The GaAs layer underneath the AlAs was doped n type at 3×10^{16} cm^{-3} with Se and was about 3 μm thick. The doping in this layer was estimated during growth from the growth parameters and confirmed with C-V profiles. The AlAs layer was estimated from growth parameters to be about 2500 Å thick and doped with Se at about 3×10^{16} cm^{-3}.

For sample 2, the GaAs top layer was 1 μm thick and was doped degenerately n type with Se at about 3×10^{18} cm^{-3}. The AlAs layer and the GaAs layer beneath it were not intentionally doped. C-V profiles of the GaAs layer showed it to be doped n type at 7-8×10^{15} cm^{-3}. The GaAs layer was about 3 μm thick. Doping in the AlAs is unknown. The AlAs thickness was estimated from growth parameters to be about 4000 Å.

Photolithographic techniques were used to define Au/Ge contacts with diameters ranging from 70 to 450 μm. Contacts were isolated from each other by wet etching using a 4:1:1 solution of H_2SO_4, H_2O_2, and H_2O. Ohmic contacts were made to the top and bottom of the samples by evaporation of an Au-Ge alloy and annealing for 20–30 s at about 400 °C. Prepared samples were then attached to TO-5 transistor headers, using conductive silver paint. Electrical connections to measurement circuitry were made using gold wire probes.

C-V measurements were made using a Hewlett Packard HP-4192 LF impedance analyzer. The analyzer was capable of monitoring the phase angle of the measured impedance. The phase angle was monitored during the data acquisition process. The analyzer was computer controlled with a Hewlett Packard 9816 computer. Data were acquired digitally, with a resolution of about 0.05 V and an effective sweep rate of about 0.083 V/s. Low-temperature measurements were made, using an MMR Technologies refrigeration station. When data were taken under illumination, the illumination source was an incandescent lamp.

We now discuss the features observed in C-V curves of the devices described. In the figures shown, forward bias denotes positive voltage on the top layer of degenerately doped GaAs. Reverse bias refers to negative voltage on the top layer. Capacitances are quoted per unit area in units of nanofarads per square centimeter. Data presented in the figures were taken in 1 MHz. The AlAs-GaAs interface refers to the interface between the AlAs and the low doped GaAs layer.

In Fig. 1 we present data for samples 1 and 2. General features of these data include hysteresis for data taken without illumination. With illuminations, no hysteresis is present, and an enhanced peak is observed. For reverse biases in excess of about 4 V, all C-V curves look more or less the same. Depletion is exhibited to the breakdown voltages of the devices, which ranged from 15 to 25 V for sample 1 and from 40 to 50 V for sample 2. One can conclude from this that no inversion occurs in this structure. This is because minority carriers are not well confined by the barrier posed

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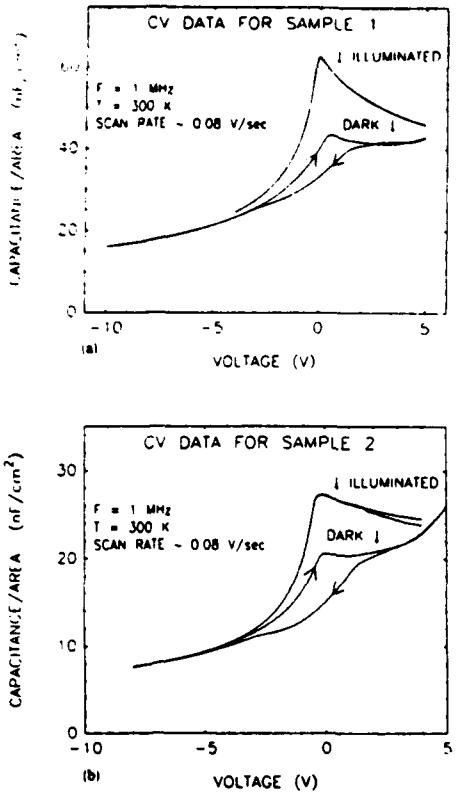

FIG. 1. (a) C-V data for sample 1. The direction of sweep is indicated by arrows. The curve of large capacitance is comprised of two curves, one for both bias sweep directions, and was taken under illumination. (b) Similar data for sample 2. All data taken at room temperature.

by the valence band of the AlAs[1].

At forward biases, one observes some leveling off of the C-V curve. This is due to accumulation of electrons at the AlAs barrier. The capacitance at this bias is roughly that of the AlAs barrier according to the formula

$$C = \epsilon/d,$$

where ϵ is the dielectric constant of AlAs and d is the thickness of the AlAs.

Further application of forward bias causes the capacitance to rise due to depletion of the AlAs barrier and conduction through the structure.[1] Forward conduction at 300 K began to be observed at about 6 V for sample 1 and about 5 V for sample 2. At 77 K, sample 1 showed evidence of conduction at about 8 V. This was determined by monitoring the phase angle of the impedance.

Near zero bias, hysteresis is evident in the C-V curves taken without illumination, with the lower branch being due to the negative going sweep. The hysteresis indicates nonequilibrium between the heterostructure and the applied voltage. This behavior can be explained by the presence of deep electron trap levels spatially localized near the AlAs-GaAs interface. It is due to the fact that at large forward biases deep levels are filled and thus neutral. At large reverse biases, deep levels are empty and, thus, positively charged. Near zero bias, the C-V curve will be different, depending upon which of these conditions initially prevailed. The lack of such hysteresis has been used as evidence for the absence of deep levels in similar structures.[7]

Consider the case when voltage is swept from reverse to forward bias. Initially, the trap levels are empty, positively charged. As the voltage is swept toward positive biases, the capacitance rises because the depletion width shrinks. Trap levels remain empty until the depletion edge nears their spatial position. The number of empty traps is out of equilibrium with the applied voltage. This is because the number of electrons near the traps is not significant until the depletion edge, which is smeared out over a few extrinsic Debye lengths,[8] nears the spatial location of the traps. As this happens, they begin to fill and become neutral. This necessitates additional depletion of free carriers and a consequent decrease in capacitance. Capacitance stops dropping when the traps levels return to equilibrium with applied bias.

Now, consider the case when voltage is swept from forward to reverse bias. Initially, the trap levels are full, neutral. Near zero bias the depletion region sweeps over the filled traps, and the number of filled traps is out of equilibrium with applied bias. This means that the capacitance will be lower than when bias was swept the other direction. Furthermore, there will be no peak in the capacitance because the thermal emission process, governing the emptying of the deep levels, will cause the return to equilibium to be slower than when bias is swept forward.

In Fig. 2 we present a C-V curve for sample 1 taken point by point. One would expect that for slow enough bias steps, an equilibrium C-V curve would be achieved, with no hysteresis. This is the case, but the time necessary to reach equilibrium is quite appreciable. C-V curves were taken with a 5-min wait between points taken 0.5 V apart, and a small hysteresis was still observed. The leveling off of the capacitance in forward bias is more pronounced in these curves than in those of Fig. 1.

In Fig. 1, we also present data taken under illumination for both samples 1 and 2, in addition to the nonilluminated data already discussed. When light is present, a nonthermal means of emptying traps is provided. No hysteresis is observed in C-V curves taken now. The fact that a peak continues to be observed can be explained as follows. The concentration of filled traps is related to the number of electrons

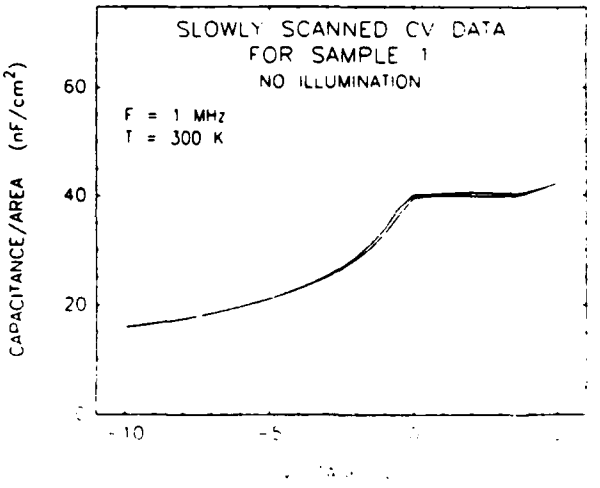

FIG. 2. Slow scan of sample 1 at room temperature. The resolution is 0.5 V with a 5-min wait between points of scan. Voltage was swept in both directions. Note the decrease of hysteresis.

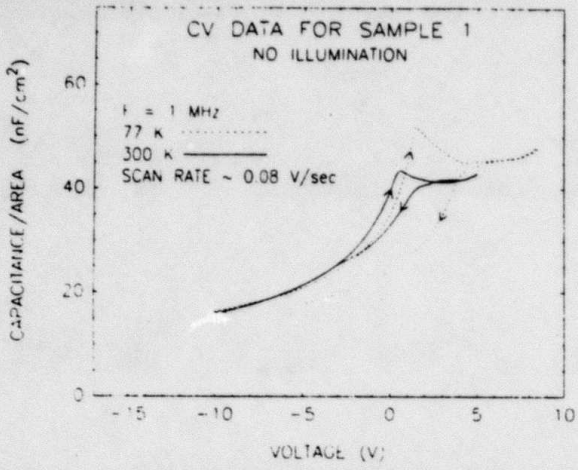

FIG. 3. C-V curves for sample 1 at 300 and 77 K. Note the increase in hysteresis for 77 K curve and the shift of the peak to more forward bias. The direction of sweep is indicated by arrows.

available to fill them, and more electrons are available when the depletion edge crosses the position of the traps. The capacitance must, therefore, continue to exhibit a peak when swept from reverse to forward bias. When swept the other direction, the peak is seen as well because light provides a nonthermal means for traps to empty. This is why no hysteresis is evident in the C-V curves when they are obtained under illumination. The overall capacitance is higher because light produces additional charge in the depletion region, thus allowing a smaller depletion width than before and a consequent increase in capacitance.

In Fig. 3 we present C-V data for sample 1 at 300 and 77 K. As temperature is decreased, the hysteresis described above increases. Additionally, the peak in the forward going curve is shifted to more positive voltage and is more pronounced. This is due to the fact that as temperature is lowered, the trap emission rate decreases, and the depletion edge becomes more sharply defined since the Debye length is proportional to $T^{1/2}$.

For sample 1, the hysteresis effect was investigated as a function of frequency at room temperature in the dark. The hysteresis effect was seen to remain almost constant for ac oscillator frequencies ranging from 10 kHz to 5 MHz. In fact, the entire C-V curve was changed very little by varying the measurement frequency.

Structures similar to those described here have been fabricated by molecular beam epitaxy (MBE). Several authors have studied these samples.[1-3] The C-V behavior of these structures is one of the properties studied. One author[1] reports on two samples which have oxygen-doped $Al_{0.5}Ga_{0.5}As$ barriers of 2000 and 5000 Å thicknesses. A lack of inversion is observed in the C-V curves of both samples. A very small amount of hysteresis near zero bias, together with a rise in forward bias capacitance, is reported for the thinner sample. Of the cited studies, these samples are the most similar to those reported here. The other two studies[2,3] are of thin barriers (about 500 Å). They do not present C-V curves taken over as wide a voltage range as that reported here. Thus, they make no comment about inversion. One paper[3] uses metal-oxide-semiconductor (MOS) theory to describe the C-V near zero bias over a wide range of temperatures (no hysteresis is observed in this study). They further report only 2% variation in experimental C-V curves as frequency is varied from 10 kHz to 1 MHz.

It is important to realize that there are differences between this report and existing studies of MBE structures. None of the studies of MBE structures present illuminated C-V curves. Data acquisition rates of dark curves are seldom given. These are important for interpretation of hysteresis in the C-V. Finally, the cited MBE studies present C-V and I-V data, as well as other measurements, while this study concentrates on capacitance behavior.

The GaAs-AlAs-GaAs structure studied in this letter exhibits a number of interesting properties in its capacitance. There is no constant capacitance region in the C-V curve in reverse bias, thus indicating that there is no inversion. There is a photosensitive region of the C-V curve near zero bias, which displays hysteresis when studied in darkness. This behavior is explained by the presence of deep levels spatially localized near the AlAs-GaAs interface.

These results can have significant implications for electronic devices fabricated by MOCVD techniques. For example, a modulation-doped structure, such as a high electron mobility transistor (HEMT), could be severely impacted by the presence of a large number of electron trap levels near the conducting channel of the transistor. The trap levels can act as a mechanism to remove electrons from the channel, decreasing the efficiency of the device. Furthermore, the fact that no inversion is observed could be detrimental to the fabrication of p-type channel field-effect transistors, using MOCVD techniques.

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PAPER 11

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OBSERVATION OF RESONANT TUNNELING THROUGH GaAs QUANTUM WELL STATES CONFINED BY AlAs X–POINT BARRIERS

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PAPER 11

ABSTRACT

Experimental evidence of resonant tunneling via quasi–stationary states confined by AlAs X–point potential energy barriers is reported in GaAs/AlAs double barrier heterostructures grown in the [100]– direction. The quantum well energy levels giving rise to the negative differential resistances observed in the current–voltage characteristics are identified by calculating the energy band diagrams of the structures. These resonant energy levels correspond to states confined in the GaAs well not only by the AlAs Γ–point potential energy barriers but also by the AlAs X–point barriers. The quasi–bound X–states are associated with the large longitudinal effective mass in AlAs corresponding to the direction perpendicular to the heterojunction interfaces.

Resonant tunneling through two $Al_xGa_{1-x}As$ quantum barriers separated by a GaAs quantum well is the object of considerable theoretical and experimental work.[1-8] Most studies are performed on structures having direct band gap $Al_xGa_{1-x}As$ barrier layers. As a result, resonant tunneling occurs via quasi–stationary states in the GaAs quantum well which are bound by the $Al_xGa_{1-x}As$ Γ–point potential energy barriers. Even when $Al_xGa_{1-x}As$ is indirect, it is often assumed that the symmetry point to consider in the barriers should be the Γ–point. However, recent experimental and theoretical studies have indicated that indirect band gap tunneling could be important in heterostructures in which the barrier layers are made of indirect band gap materials.[9-11]

This letter presents a study of resonant tunneling through GaAs/AlAs double barrier heterostructures grown in the [100]–direction. For each sample discussed, the quasi–stationary energy levels in the GaAs quantum well which produce the negative differential resistances observed in the experimental current–voltage (I–V) characteristics are identified. This is achieved by calculating the energy band diagrams of the heterostructure.[12] Energy band profiles are important in determining the actual shapes of the potential energy barriers through which the electrons tunnel. Furthermore, they give the voltage drop distributions not only in the quantum barriers and well but also in the cladding layers. These distributions may differ significantly from those based on the usual assumption that the entire applied voltage drops linearly across the barriers and well. As a result, energy band diagrams are essential in finding the positions of the resonant states in the quantum well and in identifying the origin of the negative differential resistances observed experimentally. Some of these are found to be inconsistent with energy levels confined by the AlAs Γ–point potential energy barriers. However, they can be accounted for by considering tunneling via resonant states bound by the AlAs X–point potential energy barriers.

The validity of the theoretical approach used to identify the resonances producing the experimental negative differential resistances was first tested for structures having

direct $Al_xGa_{1-x}As$ barrier layers.[12] In this instance, the peaks in current obtained in the low voltage regions of the I–V curves may be attributed without ambiguity to resonant tunneling via quasi–bound Γ–states in the GaAs quantum well.[8] In this letter, the same model is applied to two GaAs/AlAs double barrier heterostructures. Both samples were grown by metalorganic chemical vapor deposition (MOCVD) on [100]–oriented n^+–GaAs substrates.

In sample A, the GaAs electrodes are doped n–type with Se, at $1.5 \times 10^{18} cm^{-3}$ in the top cladding layer and $1.3 \times 10^{18} cm^{-3}$ in the electrode adjacent to the substrate. The AlAs layers are doped p–type with Mg at $6 \times 10^{17} cm^{-3}$. Transmission electron microscopy (TEM) measurements determined that the nominally undoped GaAs well is 45 Å wide. The AlAs barrier closer to the substrate is 71 Å thick. The other barrier is 85 Å thick. This asymmetry in barrier thicknesses should cause a given resonance in the well to be manifested at a larger applied voltage in forward bias than in reverse bias ($|V_a^F| > |V_a^R|$). For the structures discussed in this letter, reverse bias ($V_a < 0$) corresponds to a negative voltage applied to the top GaAs electrode with respect to the substrate. Fig.1 shows an experimental I–V characteristic at 4.2 K for a circular device, 50 μm in diameter. Two weak negative differential resistances exist in each bias direction. In forward bias, the peaks in current occur at $V_1^F = 240$ mV and $V_2^F = 530$ mV. In reverse bias, they take place at $V_1^R = -200$ mV and $V_2^R = -480$ mV. The I–V curve also reveals that resonant tunneling is initiated at approximately ± 100 mV. To calculate the resonant states in the GaAs well confined by the AlAs Γ–point potential energy barriers, the effective mass in AlAs is taken to be $m_\Gamma^* = 0.15\, m_0$[13], and the conduction band offsets at the heterojunction interfaces are assumed to be 1.0 eV.[14] Using these values, two quasi–bound Γ–states are found in the unbiased structure, at energies $E_1^\Gamma = 125$ meV and $E_2^\Gamma = 517$ meV above the conduction band edge at the middle of the well. To obtain the states confined by the AlAs X–point potential energy barriers, the conduction band offsets are assumed to be

0.19 eV.[14] When the large longitudinal X-point electron mass $m^*_{X_l} = 1.1\,m_0$ is used in the barriers, one quasi-stationary state, $E_1^X = 30$ meV, is found in the GaAs well. The level associated with the small transverse electron mass $m^*_{X_t} = 0.19\,m_0$ has an energy $\epsilon_1^X = 59$ meV from the bottom of the well. Two energy band profiles for the structure are depicted in Fig.2. They correspond to reverse biases of -200 and -480 mV, respectively. Both Γ- and X-point conduction band edges are shown in the AlAs barriers. The energy band diagram illustrated in Fig.2(b) indicates that in reverse bias, E_1^Γ coincides in energy with $E_c^l(x = 0)$, the conduction band edge in the left GaAs electrode at the first heterojunction interface, when $V_a = -480$ mV. Similarly, energy band profile calculations predict that the peak in current due to E_1^Γ should occur in forward bias at $V_a = 530$ mV. These values correspond precisely to the negative differential resistances observed in Fig.1 at V_2^R and V_2^F, respectively. The peaks in current at $V_1^R = -200$ mV and $V_1^F = 240$ mV should then necessarily correspond to a quasi-stationary state confined by the AlAs X-point barriers. Fig.2(a) reveals that E_1^X lines up with $E_c^l(x = 0)$ when $V_a = -200$ mV. Similarly, the peak in current associated with E_1^X is anticipated in forward bias at $V_a = 240$ mV. Energy band diagrams also indicate that resonant tunneling via E_1^X should be initiated at -90 and 110 mV in reverse and forward bias, respectively. These results are in good agreement with the experimental data. It may thus be concluded that the negative differential resistances obtained in the I-V characteristics of sample A correspond to E_1^X, the quasi-stationary X-state associated with the large longitudinal X-point effective mass in the AlAs barriers, and E_1^Γ, the lower quasi-bound Γ-state.

These concepts are illustrated on another double barrier heterostructure with pure AlAs barrier layers. In sample B, the GaAs electrodes are doped n-type with Se at $1.75 \times 10^{18} cm^{-3}$. The nominally undoped GaAs quantum well is 62 Å wide. As in sample A, the AlAs layers are doped p-type with Mg at $6 \times 10^{17} cm^{-3}$. The barrier closer to the substrate is 51 Å thick, whereas the one adjacent to the top electrode is only 42 Å

thick. As a result of this asymmetry, a given resonant state in the well is manifested at a larger applied voltage in reverse bias than in forward bias ($|V_a^R| > |V_a^F|$). The low temperature *I–V* characteristic shown in Fig.3 reveals that the first peaks in current occur at $V_1^F = 135$ mV in forward bias and $V_1^R = -140$ mV in reverse bias. Other resonances appear at 650 and −750 mV. The temperature dependence of the *I–V* curves further suggests that the broad negative differential resistance regions observed at $|V_a| < 280$ mV may actually correspond to two resonant states. At room temperature, inflections are visible at about ± 140 mV. As the temperature, T, is decreased, the low voltage regions of the *I–V* curves ($|V_a| < 140$ mV) remain almost identical, while the background current decays rapidly for larger values of $|V_a|$. As a result, the negative differential resistances become more pronounced. When T ≈ 200 K, two new small peaks appear at about ± 240 mV, next to the existing peaks at ± 140 mV. As T is further reduced, all the peaks become more prominent. This temperature dependence is illustrated in the insert of Fig.3. The energy band diagrams of the heterostructure and the quasi–stationary levels in the well may be calculated as for sample A. Three quasi–bound Γ–states are found, at energies $E_1^\Gamma = 78$ meV, $E_2^\Gamma = 325$ meV and $E_3^\Gamma = 730$ meV from the conduction band edge at the middle of the well in the unbiased structure. The energies of the two resonant X–states corresponding to the large longitudinal AlAs X–point mass are $E_1^X = 22$ meV and $E_2^X = 165$ meV. The quasi–stationary X–states associated with the small transverse AlAs X–point mass are found at energies $\epsilon_1^X = 42$ meV and $\epsilon_2^X = 176$ meV above the bottom of the well. Energy band profiles reveal that when $V_a = -140$ mV (−250 mV), E_1^X (E_1^Γ) coincides in energy with $E_c^l(x = 0)$. In forward bias, the same would occur at 135 mV (240 mV). Comparing these values to the experimental results depicted in Fig.3 suggests that the broad negative differential resistance regions observed in the *I–V* characteristics at $|V_a| < 280$ mV arise from tunneling via the two resonant states E_1^X and E_1^Γ. Since the difference in energy between these two levels is slightly smaller than the Fermi energy in the bulk electrodes, E_1^X and E_1^Γ are not properly resolved. Energy band diagrams further

indicate that the small current peaks obtained in Fig.3 at 650 and −750 mV are due to resonant tunneling via E_2^X. It may thus be concluded that the I–V characteristics of sample B reveal resonant tunneling via the first quasi–bound Γ–state, E_1^Γ, and the two X–states E_1^X and E_2^X, corresponding to the large longitudinal AlAs X–point effective mass. Energy band profiles also indicate that since E_1^X lies below the Fermi level at zero bias, resonant tunneling via E_1^X is initiated as soon as a voltage is applied. As a result, the experimental zero–bias resistance is small and the portions of the I–V curves corresponding to $|V_a| < 140$ mV remain almost independent of temperature.

The objective of this study was to identify the resonant energy levels producing negative differential resistances in the I–V characteristics of GaAs/AlAs double barrier tunnel structures grown by MOCVD in the [100]–direction. This was achieved by comparing the experimental I–V data to results obtained from the calculated energy band diagrams of the heterostructures. The main results may be summarized as follows. (*i*) Energy band profiles are essential to properly account for the voltage drops in all the layers, and to correlate without ambiguity the experimental negative differential resistances with the resonant states in the quantum well. (*ii*) Resonant tunneling via quasi–stationary Γ–states alone is inconsistent with the experimental I–V characteristics. (*iii*) The experimental data may only be explained by tunneling via resonances in the well confined by the AlAs X–point potential energy barriers in addition to resonant tunneling via states bound by the AlAs Γ–point potential energy barriers. (*iv*) The quasi–bound X–states which have been identified correspond to the large longitudinal X–point electron mass in AlAs, and not to the small transverse effective mass. This indicates that tunneling through the AlAs band gap at the X–point arises from the coupling of virtual AlAs X–point states to GaAs Γ–point states due to the breaking of translational symmetry in the direction perpendicular to the heterojunction interfaces.

In conclusion, it may be anticipated that the dominant low temperature current trans-

port mechanisms in GaAs/$Al_xGa_{1-x}As$ double barrier heterostructures in which the barrier layers are made of indirect band gap alloys are tunneling via resonant Γ– and X–states in the GaAs quantum well.

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FIGURE CAPTIONS

FIG. 1. Experimental I–V characteristic at 4.2 K for a circular device, 50 μm in diameter, fabricated on sample A. Sample A is a GaAs/AlAs double barrier heterostructure in which the nominally undoped GaAs quantum well is 45 Å wide. The doping densities in the n–type GaAs electrodes are slightly asymmetric: $1.5 \times 10^{18} cm^{-3}$ in the top cladding layer and $1.3 \times 10^{18} cm^{-3}$ in the electrode adjacent to the substrate. The barrier layers are doped p–type with Mg at $6 \times 10^{17} cm^{-3}$. The AlAs barrier closer to the substrate is 71 Å thick. The other barrier is 85 Å thick.

FIG. 2. Calculated Γ–point (solid lines) and X–point (dashed lines) conduction band edges, for the same heterostructure as in Fig.1 (sample A). (a) and (b) correspond to applied biases of −200 and −480 mV, respectively. The Fermi level in the left (right) GaAs electrode is E_f^l (E_f^r). The conduction band discontinuities at the heterojunction interfaces are 1.0 eV at the Γ–point and 0.19 eV at the X–point. In the GaAs quantum well, E_1^Γ (solid line) denotes the first quasi–bound Γ–state, and E_1^X (dashed line) is the resonant X–state corresponding to the large longitudinal AlAs X–point electron mass in the direction perpendicular to the interfaces.

FIG. 3. Experimental I–V characteristic at 4.2 K for a circular device, 20 μm in diameter, fabricated on sample B. Sample B is a GaAs/AlAs double barrier heterostructure in which the nominally undoped GaAs quantum well is 62 Å wide. The GaAs electrodes are doped n–type with Se at $1.75 \times 10^{18} cm^{-3}$. The AlAs barrier layers are doped p–type with Mg at $6 \times 10^{17} cm^{-3}$. The barrier closer to the substrate is 51 Å thick. The barrier adjacent to the top electrode is 42 Å thick.

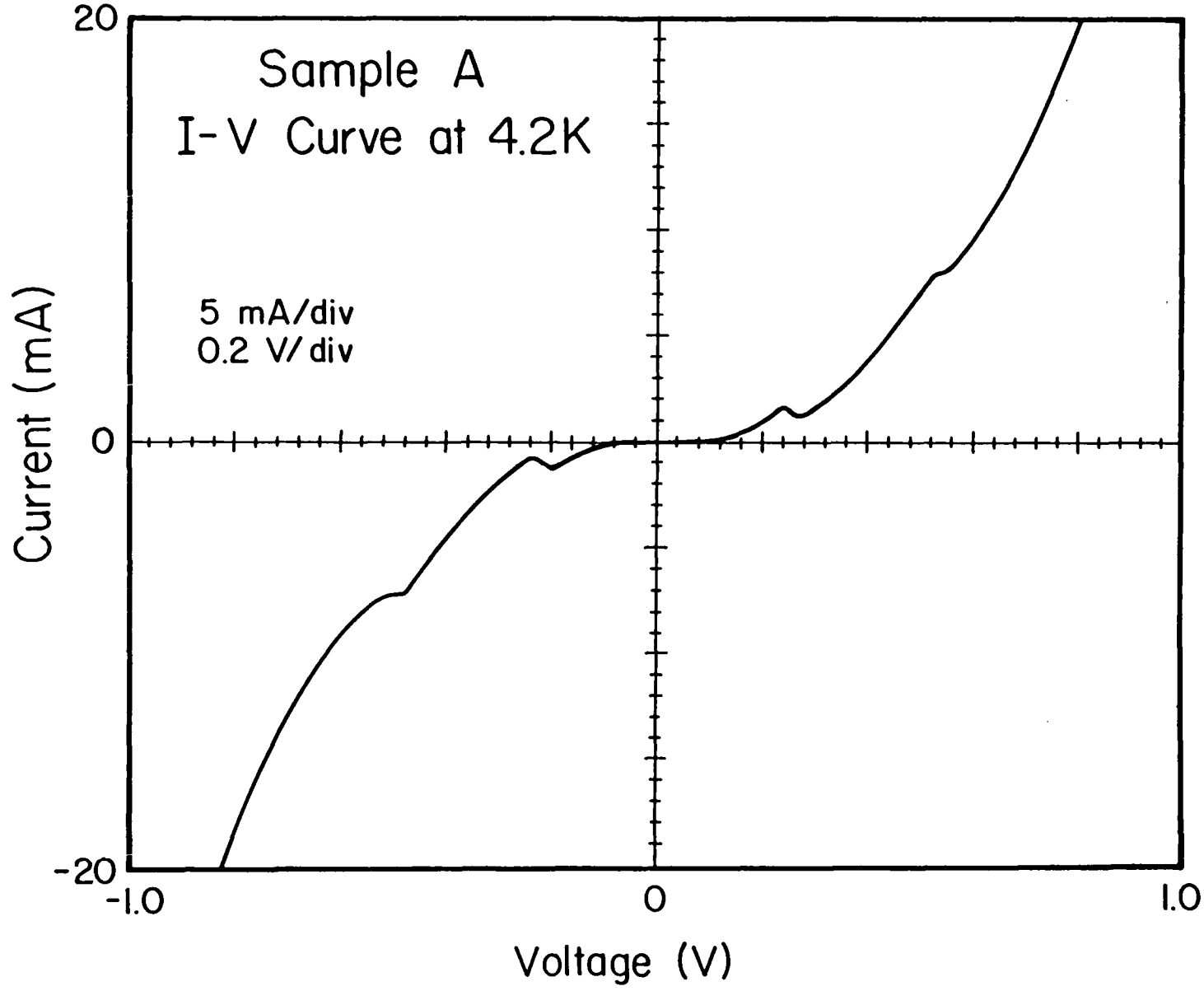
Sample A
I-V Curve at 4.2K
5 mA/div
0.2 V/div
20
0
-20
-1.0
0
1.0
Current (mA)
Voltage (V)

Figure 1

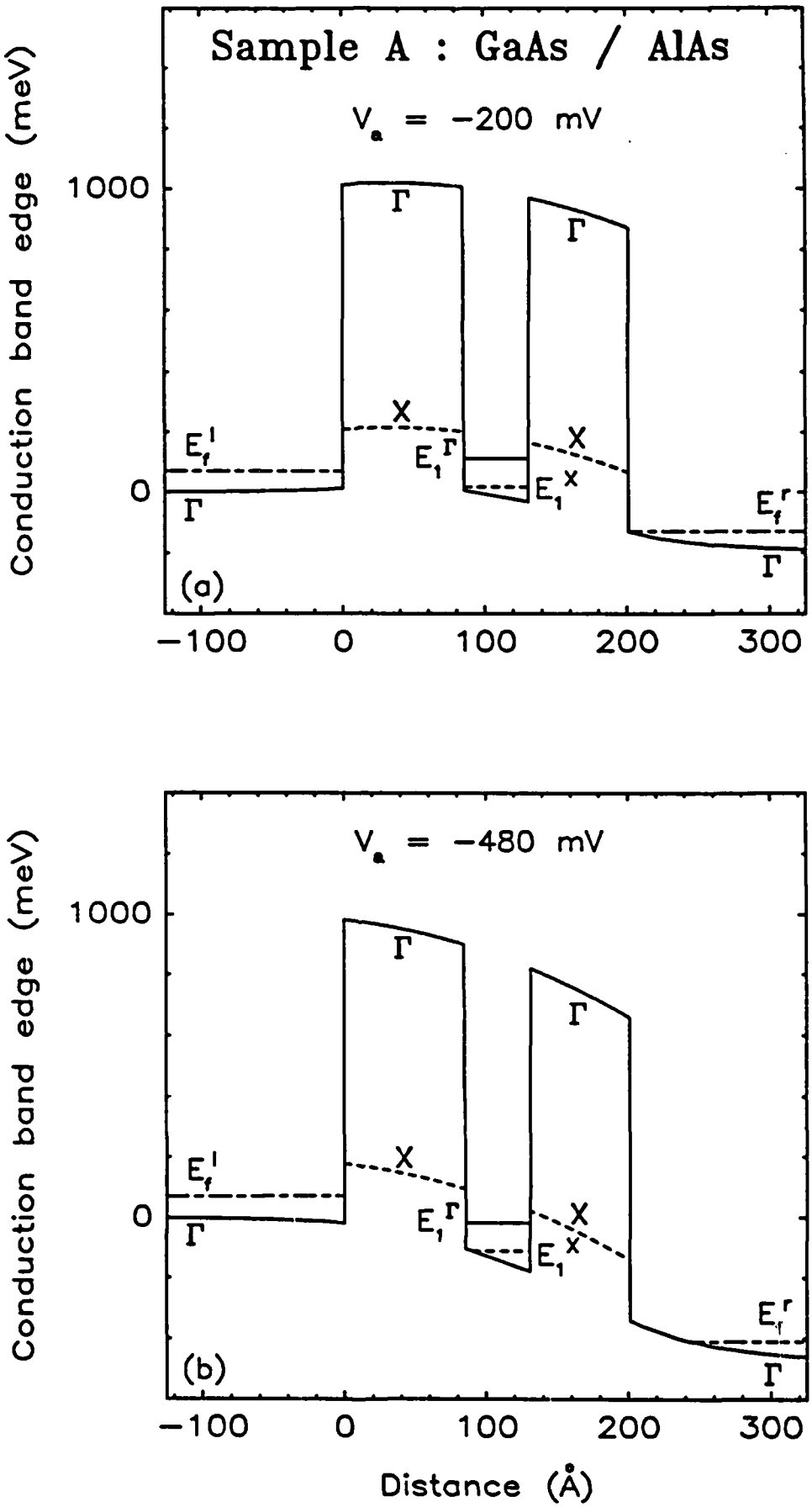

Figure 2
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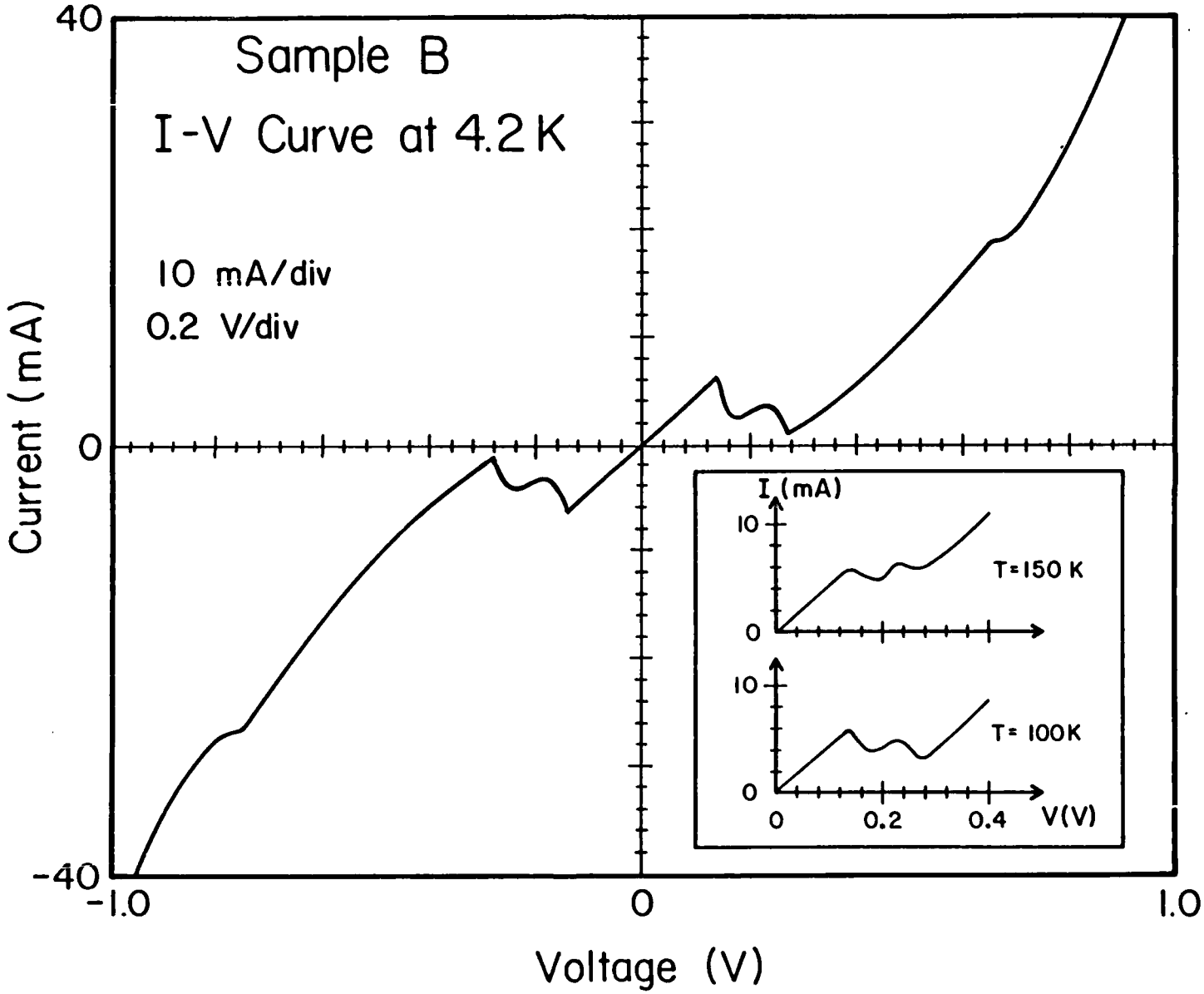
Sample B
I-V Curve at 4.2 K
10 mA/div
0.2 V/div
Current (mA)
40
0
-40
-1.0
0
1.0
Voltage (V)
I (mA)
10
0
T=150 K
10
0
T= 100K
0
0.2
0.4
V(V)

Figure 3